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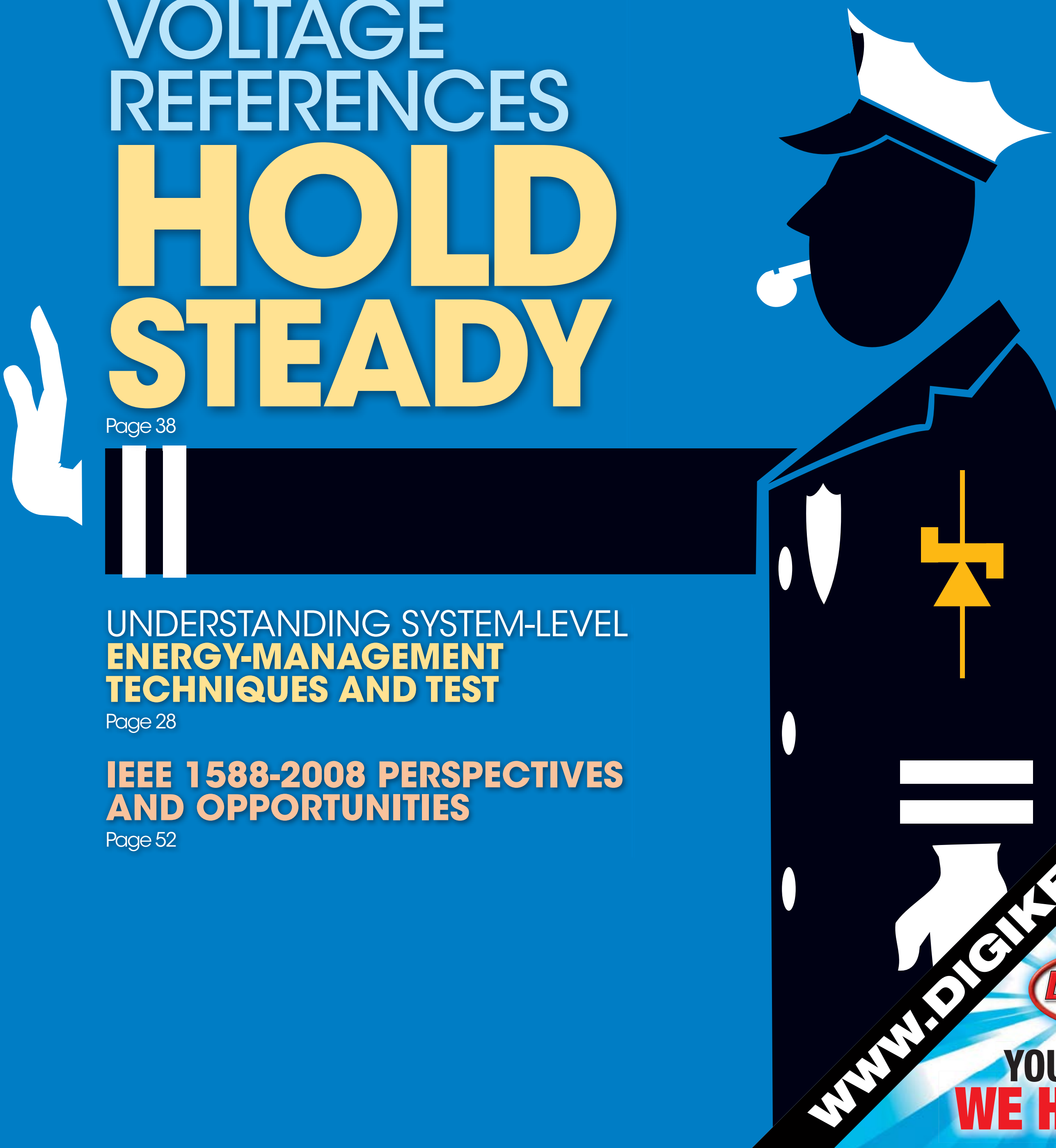

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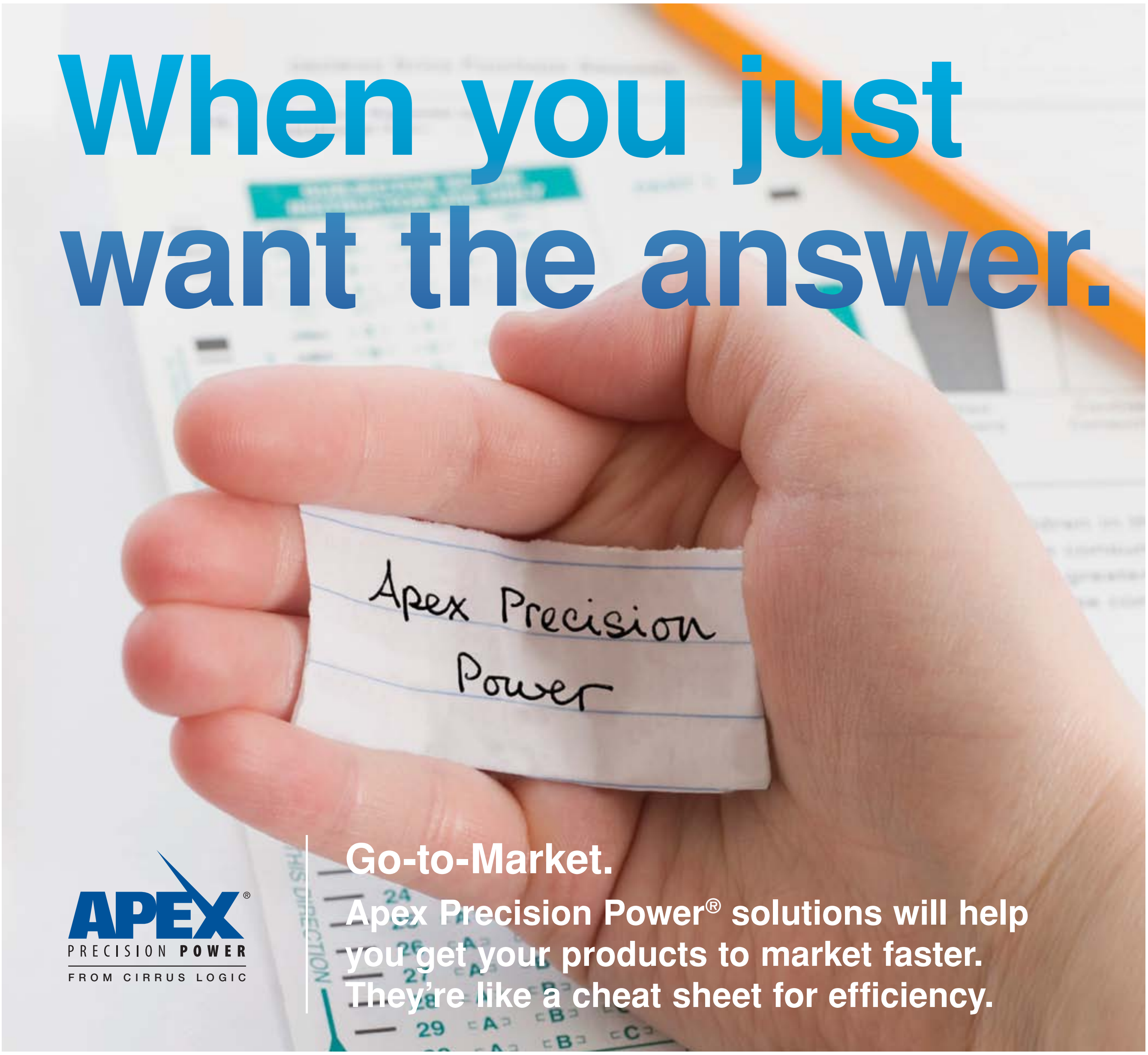

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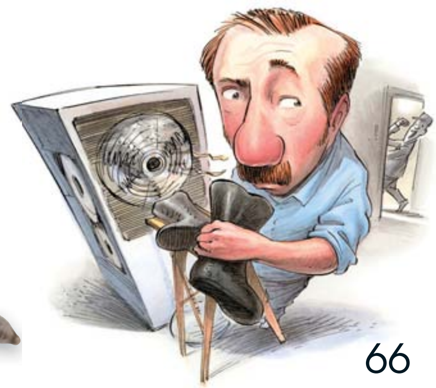
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Volume 55, Number 20 (Printed in USA).

BY BRIAN DIPERT, SENIOR TECHNICAL EDITOR

Apple's iOS and computing's potential future, Part 2

In last issue's editorial, I commented that, with iOS, the ARM-tailored OS X derivative that currently runs on the iPad, iPhone, and iPod touch, Apple has the potential to accelerate the transition to its products, thereby cementing its resurgence over Microsoft's Windows and other competitors (**Reference 1**). That aspiration became crystal-clear when Apple more than a month ago unveiled the second-generation Apple TV. Whereas the company based the original version on an Intel CPU, an Nvidia graphics chip, and an application-tailored version of the Mac 10.4 operating system, the newer device runs iOS on Apple's ARM-based A4 CPU.

The second-generation Apple TV doesn't have an associated App Store, but most observers believe that Apple is developing one. More generally, Apple is clearly planning to leverage iOS across a diverse group of hardware platforms, including, I suspect, traditional desktop- and notebook-computing form factors.

Take the iPad as a leading-edge indicator of where Apple is headed. If you have read my reviews of the system, you might think that I'm insane to predict that its descendants and derivatives will sooner or later become competitors to traditional computers. You can't use a mouse with it, for example, you can't print from it, and its "office" suites are clunky and lacking features in numerous aspects versus its PC and Mac counterparts. You can, however, tether a keyboard to it. You can even use a mouse, if you "jailbreak" it.

These facts seem to suggest that these limitations are purely Apple's choices, not fundamental hardware limitations. Printing is coming to the platform in iOS 4.2. As for those office-suite issues, software inevitably gets beefier and better with time, right? Look at it this way: Did you predict what today's computers would be capable of doing when you first peered at a 1981-era IBM PC?

With iOS-based products, Steve Jobs, Apple's co-founder and chief executive officer, gets the complete platform control he has long yearned for. His company supplies the hardware. His company creates the operating system, the bulk of the apps for it, and the development-tool suite that others harness. This time around, Apple has cultivated a large developer community, thereby rectifying one of the fundamental issues that shaped the outcome of past Mac-versus-Windows wars, but all the software funnels through the Apple App Store, with both content control and fiscal benefits. Apple can reject an app proposal for no clear reason whatsoever, and it can yank an app from the Store under the same policy. As such, it can easily subsume others' efforts into its own software. Apple even has complete control over the advertisements coming from other companies. And, I'd argue, a critical mass of consumers will accept all of these shenanigans with little to no complaint because, in exchange, they to some degree receive the it-all-just-works simplicity that they've yearned for over years' worth of struggles with technology.

Don't get me wrong; conventional computers won't go away any time soon. But I'd wager that iOS-based devices will receive most of Apple's corporate attention in the future. I saw clear evidence of the trend at this year's Developer Conference. On the one hand, I clearly acknowledge the consumer confusion and frustration that are fueling the relocation to Apple's walled garden. Heck, I even heard distinct echoes of a similar strategy in Intel Chief Executive Officer Paul Otellini's keynote speech at the Intel Developers Forum, as he explained the reasoning behind Intel's recent purchase of McAfee. I also admire Apple's skillful vision and execution in identifying and responding to those consumer concerns.

Ultimately, however, a draconian Apple-centric future is one that I believe will be in neither the consumer's nor the tech industry's best interest. No dictator has ever been able to wield power benevolently; greed sooner or later takes hold—with negative consequences. Although consumers might feel safe and secure with their Apple-branded devices and associated services, they'll eventually rebel at the high prices and limited selection of products available from Apple-controlled distribution channels. Unfortunately, at that point, they'll be so locked into the "Apple tax" that they'll have no other choice. It's up to Apple's competitors, individually and in partnership, to ensure that this undesirable outcome doesn't occur by developing superior products and services. **EDN**

REFERENCE

1 Dipert, Brian, "Apple's iOS and computing's potential future, Part 1," *EDN*, Oct 7, 2010, pg 8, http://bit.ly/af9guN.

Contact me at brian.dipert@cancom.com.

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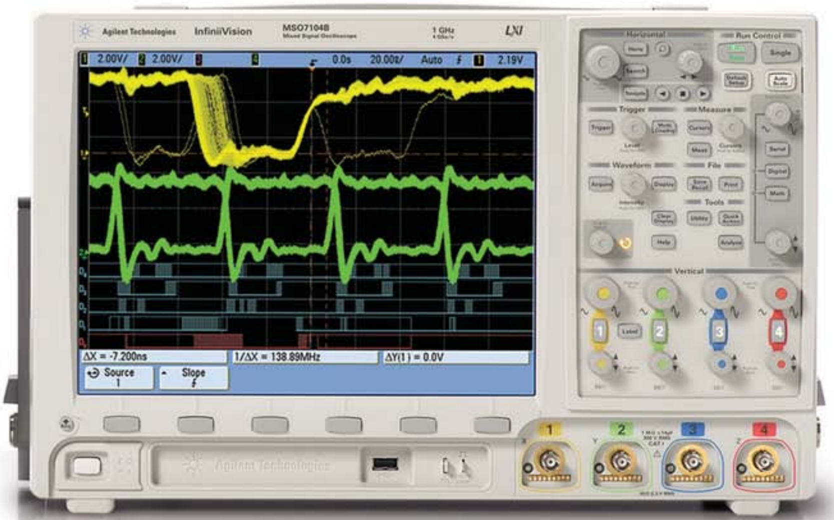

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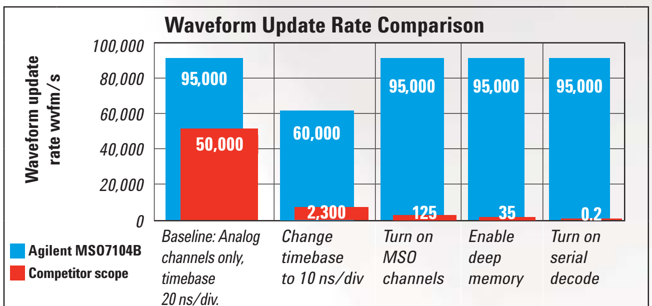

Notes: · Measurements taken on the signal using Agilent MSO7104B and a competitor's scope.
· Memory depth = display window X sample rate with up to 8 Mpts on Agilent.
· Competitor scope's test measurements taken with 2.13 firmware.

A scope's real world performance depends on more than just bandwidth and sample rates. It takes an ultra fast update rate to capture infrequent events and display the most accurate signal detail. That's where Agilent 7000B Series scopes with bandwidths from 100 MHz–1 GHz really stand out. Thanks to a proprietary chipset, you get faster update rates not only in analog mode, but in every mode. That's why you see greater signal detail. That's Agilent.

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CANON COMMUNICATIONS LLC

Time-domain-based network analyzers find 40-GHz, four-port S parameters

LeCroy Corp has announced a new class of instrument, the Sparq series of signal-integrity network analyzers. With a single button press, Sparq units measure 40-GHz S (scattering) parameters on as many as four ports at a fraction of the cost of traditional frequency-domain instruments. The new units' low prices and ease of use widen the audience for multiport S-parameter measurements. The PC-based instruments combine TDR (time-domain-reflectometry) and TDT (time-domain-transmission) technology with patented innovations to rapidly acquire waveforms and measure a DUT's (device under test's) S parameters. The Sparq measures both frequency- and time-domain results, and outputs standard Touchstone S-parameter files that are ready for loading into simulation software. The rugged, portable units include all of the hardware and software tools that signal-integrity engineers need for characterizing passive devices.

The Sparq calibrates using an internal OSLT (open-short-load-through) calibration kit, allowing automatic calibration and measurement with one button press and without connecting and disconnecting calibration standards. The unit eliminates painstaking, lengthy, error-prone calibration procedures. E-model Sparq units include both internal- and manual-calibration support using an external calibration kit. Setup uses one setup screen, which governs all S-parameter-measurement configurations. With automatic calibration, the Sparq de-embeds the attached cables, adapters, and fixture to return the S parameters of just the DUT. You need not worry about the reference-plane location or use separate software to assist in the measurements.

A standard Sparq includes all of the hardware and software tools that fast, accurate, high-dynamic-range S-parameter measurements require. You can measure single-ended, differential, and magnitude and phase S parameters and view corresponding time-domain results, including step response, impulse response, reflection coefficient, and Z normalized to a user-selectable rise time. You can also view TDR and TDT waveforms.

The Sparq software is familiar to users of the manufacturer's Windows-based oscilloscopes, sharing the same look and feel and user-friendly operation. Displays can simultaneously present as many as 16 S-parameter-result waveforms, with the ability to zoom, reposition, and perform math and measurements on waveforms in a manner similar to that of the manufacturer's oscilloscopes. The 40-GHz, four-port Sparq-4004E includes internal calibration and has a US list price of $49,990; the 40-GHz, two-port Sparq-4002E includes internal calibration and costs $37,490; and the 40-GHz, two-port Sparq-4002M offers manual calibration and costs $24,990.—**by Dan Strassberg**

▷**LeCroy Corp**, www.lecroy.com.

TALKBACK

"I bristle at your assertion that wires are unsightly. I consider wires and antennas things of beauty. Of course, my wife does not, so guess who wins that battle?"

—Engineer Ray Mack, in *EDN*'s Talkback section, at http://bit.ly/d4qsF3. Add your comments.

The Sparq signal-integrity network analyzer uses time-domain techniques to take measurements that, with traditional frequency-domain instruments, require tedious, painstaking calibration. Although Sparq lacks the dynamic range of vector-network analyzers, its dynamic range is adequate for most signal-integrity work, and its built-in autocalibration dramatically shortens measurement times.

Improving RF Transmission Efficiency

Tiny RF PA Power Management IC

RF Power amplifiers used in cell phone applications are typically powered directly from the battery. This creates a challenge for the designers: as RF devices, the power amplifier adjusts the voltage and current based on the transmission. Inefficiencies are created when the PA supply voltage and the output voltage are different.

The MIC2808's DAC controlled adjustable voltage output feature minimizes the input to output voltage differential, thus improving efficiency and battery life. The voltage is adjusted based on real-time needs of the PA to achieve the most efficient operation at any given transmit power level.

For more information, contact your local Micrel sales representative or visit Micrel at: www.micrel.com/ad/mic2808.

Ideal for use in:

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- WiFi modules
- DECT handsets

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Mentor accelerates embedded-system design

Mentor Graphics has introduced the Mentor Embedded ReadyStart Platform, which is available in a version that uses the Nucleus operating system and another version that uses the Nucleus and Android operating systems. It combines integrated software IP (intellectual property) with tools and services to support processor-based boards and SOCs (systems on chips).

Shay Benchorin, director of marketing and strategic alliances at Mentor's embedded-systems division, says that ReadyStart quickly gets users up and running, with out-of-the-box bring-up time as low as 15 minutes. ReadyStart comes with ready-to-use demonstrations applicable to medical, industrial, automotive, and consumer devices. Benchorin cites printers; RFID (radio-frequency-identification) systems; lighting controls; LED drivers; motor controllers; HVAC (heating/ventilation/air-conditioning) pumps and compressor motors; blood analyzers and portable medical devices; surveillance, access-control, and alarm systems; and white goods as potential targets for ReadyStart-based design efforts.

ReadyStart tightly integrates Mentor's Nucleus real-time operating system with Mentor's Inflexion platform user-interface runtime engine for 2- and 3-D graphics and wired- and wireless-connectivity middleware. ReadyStart for Nucleus now supports SOCs and boards from Atmel (www.atmel.com) and Texas Instruments (www.ti.com), and Mentor plans future support for Freescale (www.freescale.com), Marvell (www.marvell.com), and other semiconductor vendors.

For multiple-operating-system applications on multicore processors, Mentor provides a version of ReadyStart that includes Android, Nucleus, Inflexion, middleware, and MCAPI (multicore-communications application-programming-interface)-compliant interoperating-system communication. The ReadyStart multiple-operating-system platform currently supports the Freescale P1022 dual-core SOC.

Mentor's embedded ReadyStart Platform for Android and Nucleus employs this user interface and enables the demonstration of a printer incorporating the Freescale P1022 chip.

Benchorin sees a trend toward the Nucleus-only approach for low-cost products. A Nucleus-only approach can minimize power consumption and enable a BOM (bill-of-materials) cost as low as $25 for a low-end set-top box.

ReadyStart complements Atmel ARM-based devices because mutual customers want an integrated hardware/software platform that addresses power-management and embedded-graphics capabilities as well as traditional stacks for communication interfaces, such as USB (Universal Serial Bus) and Ethernet, according to Jacko Wilbrink, Atmel's marketing director for ARM-based products. Mentor's customers who develop smart-home metering, industrial automation, medical, white-good-control-panel, and secure-terminal applications will realize cost savings in using the product, he says.

The ReadyStart Platform for Nucleus for a single project with two developer seats costs $24,995 and includes the Nucleus real-time operating system, wired- and wireless-connectivity middleware, and the Inflexion user-interface runtime engine. JTAG (Joint Test Action Group) probe support is also available.

—by Rick Nelson

▷**Mentor Graphics**, www.mentor.com.

DILBERT By Scott Adams

RAQ's

Rarely Asked Questions

Strange stories from the call logs of Analog Devices

Contributing Writer John Ardizzoni is a Senior Application Engineer at Analog Devices in the High Speed Linear group. John joined Analog Devices in 2002, he received his BSEE from Merrimack College in N. Andover, MA and has over 30 years experience in the electronics industry.

Is amplifier headroom cramping your style?

Q: When running on a single supply, my op amp's output is highly distorted. Could this be some kind of headroom issue?

A: Headroom is definitely one of many reasons why the output could be distorted. For those of you new to the term, headroom is a measure of how close the input and output of an amplifier can swing to the supply rails. You may also hear the term *footroom*, which refers to distance from the negative supply, but headroom commonly applies to both rails. Therefore an amplifier with ±0.8 V of headroom can swing to within 0.8 V of the supplies.

Fortunately, an amplifier's headroom requirements can quickly be determined from the datasheet specifications or performance plots. Input headroom is the difference between the input common-mode voltage range (ICMVR) and the supply voltage. Output headroom is the difference between the output voltage swing and the supply voltage. Exceeding the ICMVR or asking the amplifier to deliver more than the specified output swing will certainly distort the output signal.

Running on a single supply can further complicate matters. Just about every amplifier can be run on a single supply. The amplifier doesn't care if a single 10 V supply or dual ±5 V supplies are used; it sees 10 V across its supply pins in both cases. There is a difference at the input, however. With symmetrical bipolar supplies, the mid-supply voltage is zero; with a single supply, the mid-supply voltage is half of the supply voltage.

For ground-referenced signals, bipolar supplies are preferred because both are referenced to ground (mid-supply). In single-supply applications, the input signal must be offset to match the mid-supply voltage in order to maximize amplifier headroom and minimize power dissipation. This can be either done at the signal source or at the amplifier input. At the amplifier input, ac coupling may be required and a new mid-supply bias voltage must be established, increasing the circuit complexity.

One alternative to this problem is to use a "true" single-supply amplifier. The ICMVR of these amplifiers includes the negative rail, helping to alleviate ICMVR issues. A second alternative is to use rail-to-rail amplifiers, which have inputs and outputs that can swing within a few millivolts of the supply rails. A third alternative is to use an amplifier that includes a charge pump to internally generate the negative rail.

So if your amplifier design leaves you feeling a bit cramped, kick off your shoes and relax. There are many ways to find a little more headroom or footroom.

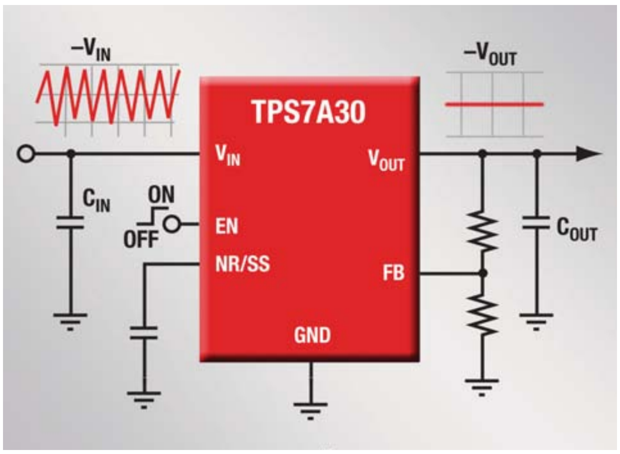
To Learn More About Amplifier Headroom
http://dn.hotims.com/27759-101

Have a question involving a perplexing or unusual analog problem? Submit your question to: www.analog.com/askjohn

For Analog Devices' Technical Support, Call 800-AnalogD

Negative-output, 36V low-dropout regulator supplies 200 mA

Texas Instruments' new TPS7A30 negative-output low-dropout linear regulator is stable with any output capacitance—ceramic or otherwise—greater than 2.2 µF. The dropout voltage is 216 mV at a 100-mA output current. The device accepts inputs of –3 to –36V. An adjustable-output version lets you set output voltages of –1.18 to –33V. Fixed versions have 1.5% nominal accuracy over load, line, and temperature. Output noise is 15.1 mV rms, and PSRR (power-supply-rejection ratio) is 72 dB at 1 kHz and 55 dB from 10 to 700 kHz. The devices have an enable pin and an NR/SS (noise-reduction/soft-start) pin, which allow you to lower noise and provide for soft start by adding a small capacitor. Maximum supply current is 3 µA in shutdown mode. Quiescent ground current ranges from 55 µA at 0A output current to 950 µA at 100-mA output.



Texas Instruments' new TPS7A30 negative-output low-dropout regulator has an enable pin and a noise-reduction/soft-start pin, which enable you to lower noise and provide for soft start by adding a small capacitor.

The regulators target use in noise-sensitive applications, such as test equipment; industrial, networking, and telecom equipment; base stations; microwave and radio links; noise filtering for receiving, transmitting, and power amplifiers; and medical equipment.

The TPS7A30 is available in MSOP-8 PowerPAD packaging, operates over –40 to +125°C, and sells for $1.50 (1000). The TPS7A30-49EVM-567 evaluation module sells for $20.

—by Paul Rako

▷**Texas Instruments**, www.ti.com.

> The regulator is stable with any output capacitance greater than 2.2 µF, and it accepts inputs of –3 to –36V.

New chip process enables wireless and power management on one IC

10.21.10

Power management is a common thread in almost all emerging applications that rely on electronics: Mobile-system applications have the limiting factor of a finite battery-power budget, whereas permanent-system applications may reside far away from ac-mains electricity and must survive on harvested energy or battery power.

However, these devices usually interact with their environments, taking input from sensors and outputting control signals to lights or energy monitoring and communicating with a network. In an effort to streamline both circuit size and component count in such applications, IBM's foundry service has introduced a high-voltage, mixed-signal process, CMOS-7HV, which allows the combination of power management and wireless power on one chip.

One example of the importance of wireless-enabled power-management chips is in Smart Buildings, in which sensor-enabled control of lighting systems can save a sizable amount of building energy. Each light needs power management, for example, to perform ac/dc or dc/dc current-regulated power management for LED luminaires, and each must also process information, such as occupancy detectors and ambient-light sensors, communicating the information back to the building's control network. Implementing the power and wireless-communications functions on one chip saves space and potentially reduces costs—both vital in retrofit lighting. Another application is in electric and hybrid vehicles, in which wireless power-management chips could cut as much as 30% from the weight of the car's wiring harnesses, an important factor in gasoline-efficient cars.

The CMOS-7HV process features 180-nm lithography; triple-gate-oxide, high-voltage-CMOS technology, including 20 to 50V FETs that are extendable to 120V; shallow-trench isolation; and 150,000 circuits/mm^2. RF features include precision poly, diffusion, and well resistors; vertical natural-MIM (metal/insulator/metal) capacitors for high-voltage use; varactors; high-voltage Schottky barrier diodes; and low-current inductors. IBM is rolling out the new chip-making process to manufacturers in the consumer-electronics, industrial, automotive, digital-media, and alternative-energy segments.

—by Margery Conner

▶IBM, www.ibm.com.

DSOs offer 20-GHz real-time bandwidth on four channels, 45 GHz on one, no noisy bandwidth fix

A few companies compete fiercely in the top-of-the-line real-time DSO (digital-storage-oscilloscope) market, but until now only one had produced a scope that achieves 20-GHz bandwidth on four channels at once.

Competitors express skepticism about that manufacturer's technique for enhancing bandwidth. The technique uses digital-signal processing to compensate for frequency-dependent attenuation that would otherwise affect components of the signal that lie above approximately one-third of the sampling frequency. However, this approach exacts a potentially crippling penalty on the performance of bandwidth-enhanced scopes: higher noise when you switch on the bandwidth enhancement.

LeCroy's four-channel WM (WaveMaster), SDA (serial-data-analyzer), and DDA (disk-drive-analyzer) scopes in the new 20-model 8Zi-A series include 10 units that each provide 20-GHz bandwidth on four channels simultaneously without resorting to the kind of bandwidth enhancements its competitor employs. As a result, LeCroy claims that, especially when you select 20-GHz, four-channel bandwidth on the units that offer it, its new scopes introduce significantly less jitter and noise than do the competitor's bandwidth-enhanced units.

The new scopes achieve their high bandwidth despite using 40G-sample/sec/channel digitizers, which are 20% slower than the 50G-sample/sec/channel units of the competitor's instruments. LeCroy notes that, as long ago as 2002, it successfully marketed a scope that, like the 8Zi-A units, sampled at just two times its –3-dB frequency. The company considers the small amount of low-frequency aliasing that can appear when you view signals containing components near the –3-dB frequency to be a reasonable price to pay for lower noise that allows a significantly more detailed view of the displayed signals. Moreover, unlike the bandwidth-enhanced scopes, 8Zi-A units that feature 20-GHz, four-channel bandwidth let you use the highest sensitivities at bandwidth settings greater than 16 GHz.

With its –3-dB frequency of 45 GHz, the WM845Zi-A claims the prize for the industry's highest real-time bandwidth. Its ability to simultaneously display four 20-GHz or two 30-GHz signals without the use of bandwidth-enhancement techniques that magnify high-frequency noise many be more important to many users, however.

The 8Zi-A series includes one WM model and one SDA model that also offer 45-GHz real-time bandwidth on one channel that effectively takes 120G samples/sec. The company achieved this performance with its proprietary DBI (digital-bandwidth-interleave) frequency-domain-based real-time-sampling technology. Previously, only sequential-sampling oscilloscopes could acquire more than 100G samples/sec/channel and achieve bandwidth greater than 30 GHz. However, sequential-sampling scopes are equivalent-time devices that cannot capture single-shot transients, and they acquire waveforms more slowly than do real-time scopes.

Several other 8Zi-A scopes also feature DBI. These instruments sample two channels at 80G samples/sec/channel and, depending on the model, provide two-channel bandwidth of 25 or 30 GHz. Two models offer both two-channel, 80G-sample/sec, 30-GHz acquisition and single-channel, 45-GHz, 120G-sample/sec modes.

In WM units, the base amount of waveform memory is 20M samples/channel, with options to increase that number to as much as 256M samples/sec/channel. In SDA and DDA models, the base waveform memory is 32M samples/sec/channel, which you can also increase to 256M samples/channel. In models that contain waveform memory of this depth and in which DBI triples the sampling rate to 120G samples/sec, the memory depth becomes 768M points, or 6.4 msec. Because the use of DBI always increases

> "The scopes use Windows 7 and a 3-GHz quad-core Pentium processor.

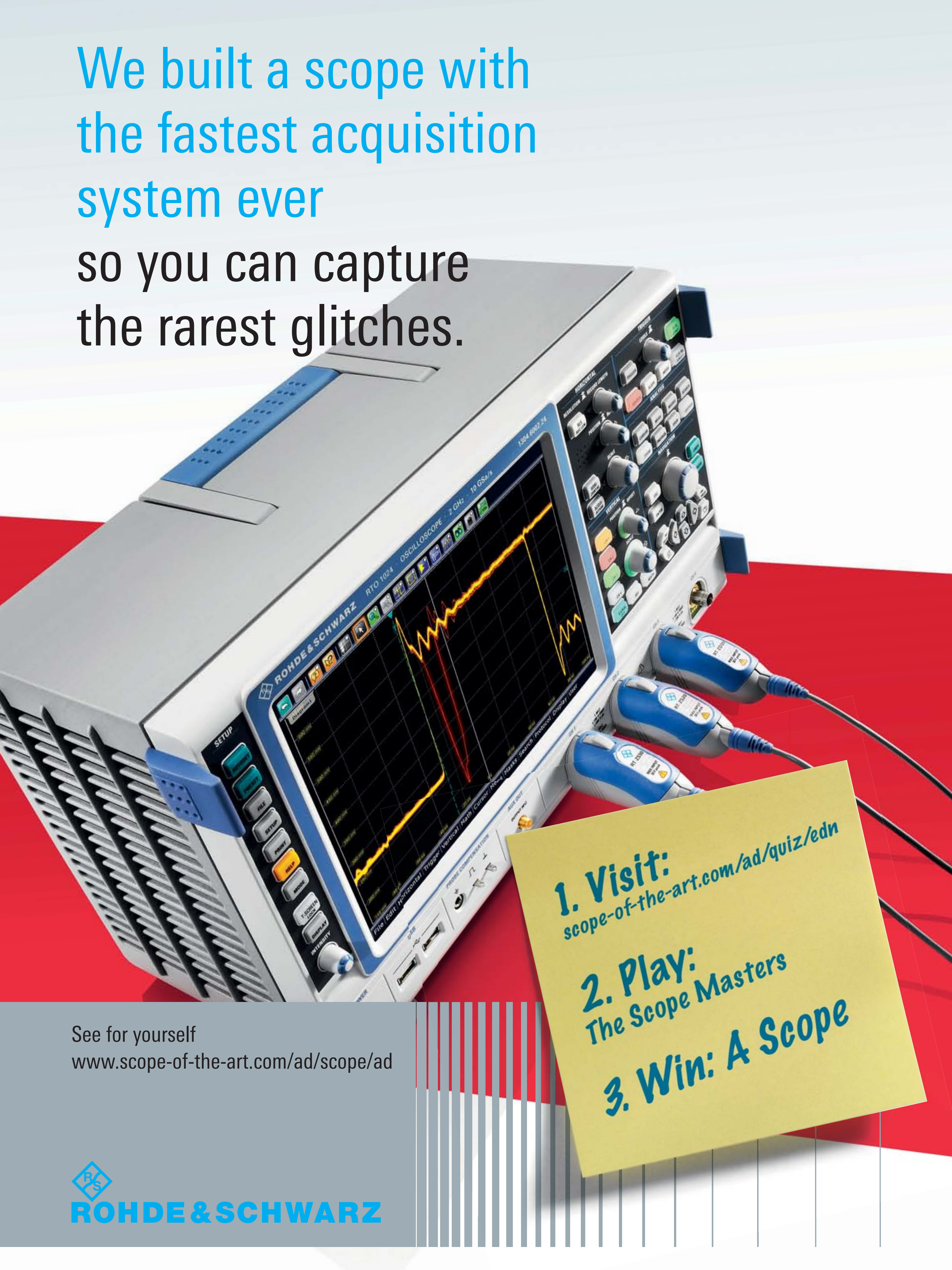
the waveform-memory depth in proportion to the sampling rate, you can also capture records of this duration at 40G samples/sec on four channels or 80G samples/sec on two channels.

Besides the 32M-sample/channel base memory, the SDA and DDA models incorporate additional analysis software that the WM models lack. However, LeCroy can upgrade any of the series' 20 models to any other that offers more features or higher performance. Technically, downgrades are also possible, but the company is not considering offering them.

The 8Zi-A units use the Windows 7 OS and a 3-GHz quad-core Pentium processor with 8 Gbytes of processor RAM, making them, according to LeCroy, the only scopes that can perform full analysis processing on the entire contents of their waveform memories. US prices for the 8Zi-A series range from $68,490 for a 4-GHz-bandwidth, 40G-sample/sec/channel WM unit to $314,000 for an SDA 45-GHz bandwidth, 120G-sample/sec/active channel SDA unit.

—by Dan Strassberg

▷**LeCroy Corp**, www.lecroy.com.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VOICES

NEDA's Robin Gray: components of opportunities and challenges

Robin Gray, Jr, executive vice president at NEDA (National Electronic Distributors Association, www.nedassoc.org), discusses the opportunities and challenges the electronics supply chain faces as it finishes 2010 and looks to 2011. An excerpt of his recent discussion with *EDN* follows. Read the complete interview at www.edn.com/101021pa.

Has the electronics supply chain recovered from 2009's economy?

A It depends on your perspective. Last year was a down year, but it wasn't an abysmal year for distributors and manufacturers of electronic components. Business was definitely off from the previous year, but it didn't go negative [as it did in] a lot of other industries. This year has been a strong growth year in sales profitability and average selling prices.

On the other hand, customers saw longer leadtimes and increasing prices. So, depending on your perspective of the supply chain, 2010 is a good year or a not so good year.

Even having said that, for a lot of sectors in 2010, business remained good. In our electronics-components industry, things looked positive compared to the overall economy.

Some leadtimes are at 20-plus weeks. Do you see supply and demand stabilizing at any time in the near future?

A Not really. A lot of companies learned the lesson of 1999/2000 and the dot-com/telecom implosion. That downturn was the biggest we had seen. The lessons we took away from that [downturn] were: Watch your inventory levels, and don't expand capacity so much that you are caught with an oversupply of inventory.

Right now, inventory levels remain lean. You don't see many manufacturers ramping up production. There is an uncertainty about where the economy is going. Most people I talk to are uncertain month to month about where things are going. I doubt that many companies want to invest in expansion to shorten leadtimes.

How does migrating manufacturing overseas impact distributors and distribution, traditionally a North America-based business?

A For all intents and purposes, that migration is over. To a certain extent, there is a movement to other low-cost regions other than China. There's little impact now. High-volume [distribution], which followed your big-time customers that did outsource or move to Asia, switched to design functions or expanding their presence overseas, whether that was through acquisition or starting up new distributors.

As for manufacturers, a lot that moved to China did so to take advantage of low-cost labor but also to get an entry into the Chinese market. With increased government regulation in China, a lot of companies are rethinking their commitment to China. If they are there only for the low-cost labor, they can go elsewhere now. If they want to stay in the market and sell into the market, then they are probably going to stay.

Movement into China has also brought some big problems to the electronics supply chain. The principal one is counterfeiting. Has there been any improvement in thwarting counterfeiting globally?

A Not in the sense that there has been much of a dent made in stopping counterfeiting. On the other side, the government and more large customers, particularly customers that sell to the military or to aerospace and aviation, have become concerned about counterfeit [products].

The government is increasingly doing things about that problem, whether it is through enforcement or mandating through regulation government-procurement practices that would prevent or minimize the risk of getting counterfeit products—and that would be first buying from authorized sources, whether that's directly from the manufacturer or from an authorized distributor.

What are the biggest market opportunities and challenges for distributors in the design chain and fulfillment as we move into 2011?

A Finding the right partnership expertise and suppliers to gain entry into emerging markets, such as alternative energy and lighting, for example. There's a learning curve that's involved, and, because a lot of these customers are not established or well-known, there's a lot of work to be done to develop those companies and find the right ones. A lot of them are going to fail, but some will emerge as winners.

Telecom infrastructure and broadband are growing strongly right now. With so many smartphones being built and so much bandwidth being needed to support that [technology], telecom companies are rapidly building their infrastructure. A lot of goods are being sold into the consumer side in smartphones and other devices, such as iPads, that are heavily using broadband access, and the telecom-company customers are buying finished goods and components to build that infrastructure.

The risk of that approach, of course, is too-optimistic forecasts by phone manufacturers that they are going to grab market share from [their competitors] or to have technology that the consumer doesn't invest in or too much expansion, which leads to a glut of inventory.

—interview conducted and edited by Suzanne Deffree

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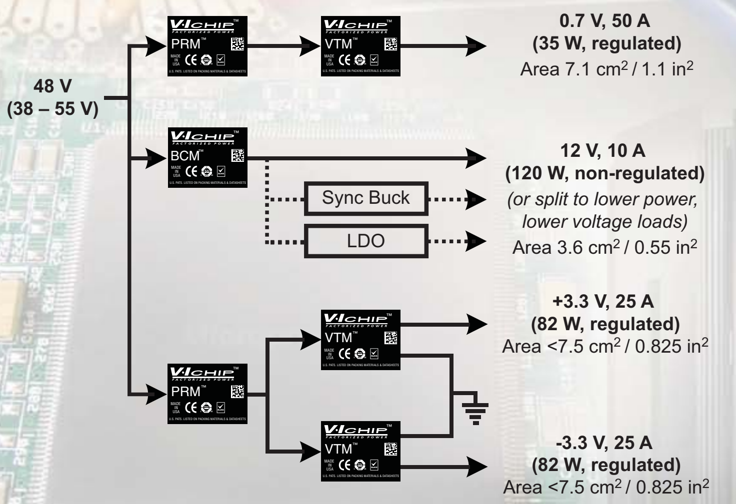

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BY BONNIE BAKER

Absorb current spikes and noise with a simple technique

When using an 8- to 14-bit ADC in your system, it is critical that you understand the voltage-reference path to the converter. **Figure 1** shows a circuit that accommodates the dynamics of the ADC's reference input. In this **figure**, the voltage-reference chip provides a voltage foundation for the conversion process and a capacitor, C_{L1}, to absorb the ADC's internal reference circuitry current spikes and filter-reference noise (**Reference 1**). It is important not only to reduce voltage-reference noise in this circuit but also to balance the stability of the internal voltage-reference amplifier.

When addressing the noise issue with this circuit, the ADC transfer function reveals the role of the voltage-reference noise, according to the following **equation**: $CODE=V_{IN}(2^N/V_{REF})$, where V_{IN} is the input voltage to the ADC, N is the number of ADC bits, and V_{REF} is the reference voltage to the ADC. The reference-voltage variable includes all errors associated with the reference chip, such as accuracy, temperature variations, and noise. In all cases, reference errors become part of the gain error of the ADC system.

You can calibrate most of these errors with the system processor or controller. If you are measuring several points from the negative full-scale to the positive full-scale of your ADC, you will see a gain error from these errors as a function of the converter's input voltage. Noise is one error that you cannot calibrate with your processor or controller. The reference noise at the output of the converter grows larger with the analog input voltage (**Figure 2**).

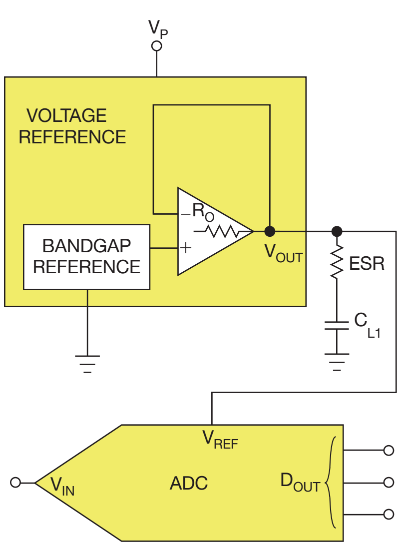

Figure 1 This circuit accommodates the dynamics of an 8- to 14-bit ADC's reference input.

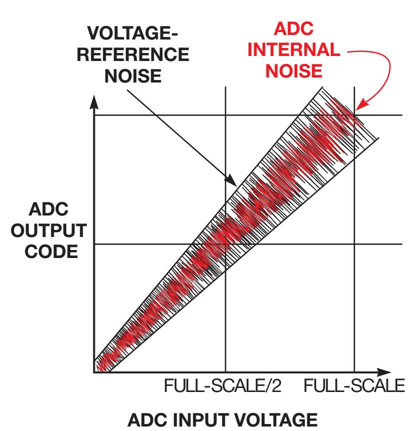

Figure 2 The reference noise at the output of the converter grows larger with the analog input voltage.

Data sheets for most voltage references have an output-voltage-noise specification over a 0.1- to 10-Hz frequency range. Some manufacturers include specifications for the voltage-reference output-noise density. This specification usually refers to noise in the broadband region, such as the noise density at 10 kHz. Regardless of how the manufacturer specifies the noise of this reference, however, an added lowpass filter reduces overall noise at the reference output. You design this filter with a capacitor and the ESR (equivalent series resistance) of the capacitor. You ensure stability in the design by using the same techniques recommended in **Reference 2**.

The accuracy of **Figure 1**'s voltage reference is important; however, you can calibrate any initial inaccuracy with hardware or software. On the other hand, eliminating or reducing reference noise while absorbing the current spikes on the ADC's reference pin requires characterization and hardware-filtering techniques.

Next month's column will investigate and design a voltage-reference circuit that is appropriate for 16-bit and greater converters. EDN

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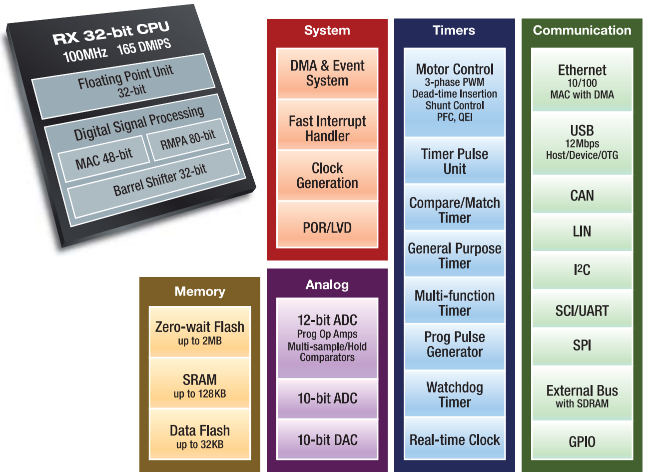

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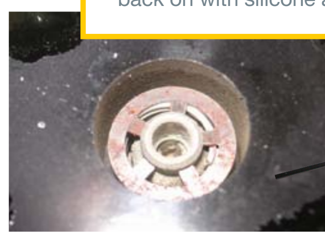
The West Bend No. 1 electric-frying-pan thermostat

About 15 years ago, I bought a Grants electric frying pan on eBay for $10. Recently, the knob of the pan's West Bend thermostat stopped turning. Knowing that putting pliers to it would only break the knob or strip the knurling, I opted instead to disassemble the unit. The threaded shaft that the knob operated had dried out and seized. Lubricating the threads with Tri-Flow fixed the thermostat. The thermostat also has a neon light that had stopped operating due to age. When I shined a bright light on the failed neon lamp, it started working again because the light preionizes some of the noble gases inside the lamp. The lamp stopped working when I reassembled the unit because it was mostly shielded from ambient light.

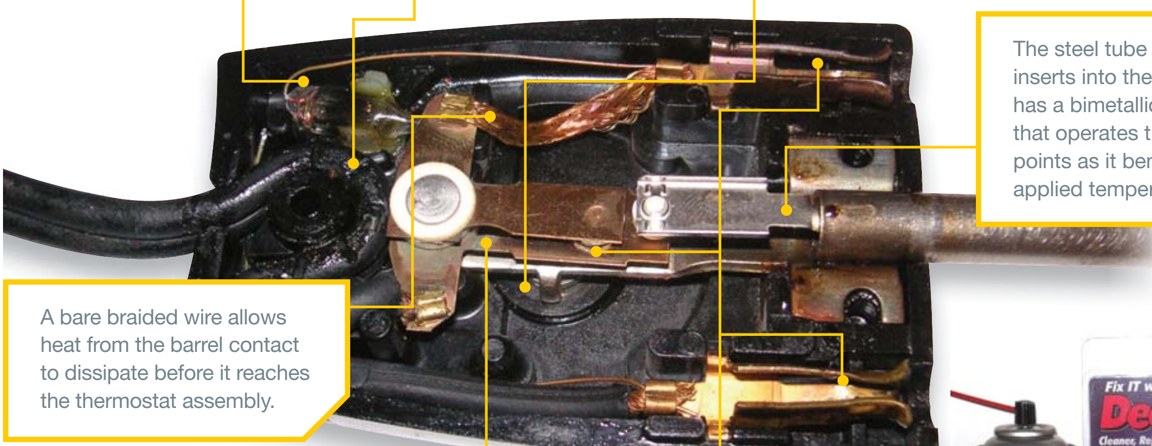
Prying off the metal label revealed a dreaded sight: a snap ring designed only to go on, not come off for service. I managed to pry the ring off with a 0.4×2×60-mm, flat-blade Stahlwille screwdriver. A spring holds the knob against the body as the central shaft moves in and out. I glued the label back on with silicone aquarium cement.



A neon light with a series dropping resistor is wired across the two output terminals so that the lamp glows when the thermostat closes and power travels to the pan's heating element.

A loop of wire over one of the three screw bosses serves as a wire-strain relief. The bottom cover has bumps that clamp the wire when it is assembled.

The knob seized because lack of lubrication caused the threads in the metal frame to seize. To free up the threads, I sprayed them with Tri-Flow spray lubricant and carefully worked the knob back and forth in small increments, using pliers when necessary. When the threads were properly lubricated, I could turn the knurled shaft with my fingers.

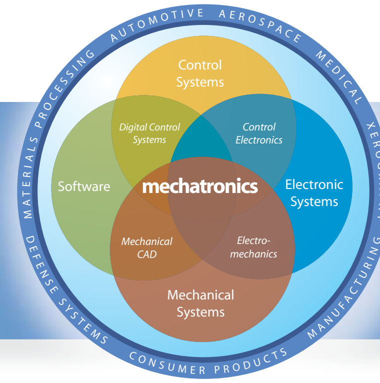


The steel tube that inserts into the frying pan has a bimetallic element that operates the contact points as it bends with applied temperature.

A bare braided wire allows heat from the barrel contact to dissipate before it reaches the thermostat assembly.

Rotating the temperature knob pushes the lower contact leaf closer to or farther from the bimetallic spring. When the lower leaf is far from the bimetallic spring, it must heat up more to bend far enough to open the contact points.

Applying a few spritzes of DeoxIT liquid on the contacts cleans, protects, and lubricates them when they engage the pins on the frying pan. I found a business card, from an honored competitor, with a good abrasive texture and cut it into strips that I ran between the contact surfaces after I applied the DeoxIT.



Control design: pervasive and perplexing

Feedback, feedforward, and a disturbance observer get the job done.

Control is a hidden, enabling technology that is present in almost every engineered system. Despite this fact, control-system design is still mysterious and often falls in the domain of a specialist. Every engineer must now know how to create, implement, and integrate a control system into a design from the start of the design process. To effectively accomplish these goals, an engineer must understand how to balance performance, low cost, robustness, and efficiency.

You can best evaluate a design concept through modeling, not through building and testing, because modeling provides true insight on which to base design decisions. A hierarchy of models of varying complexity and fidelity exists, but a simple design model—dominant dynamics—that captures essential attributes is the most useful. An integrated control system can enhance a design through stabilization, command following, disturbance and noise rejection, and robustness. You can accomplish all of these goals through a combined approach, rather than with one feedback controller.

To best understand this combined approach, I had extensive discussions with Rob Miklosovic, PhD, a leading mechatronics innovator at Rockwell Automation (Cleveland, OH). **Figure 1** illustrates the approach. The design model typically finds use in both feedback- and feedforward-controller design. However, in practice, the physical system deviates from that design model. A disturbance observer regards any difference between the physical system and the design model as an equivalent disturbance to the model. It estimates the disturbance and uses it as a cancellation signal. So in addition to enhancing disturbance rejection, the disturbance observer makes the physical system behave as the design model over a certain frequency range, thereby simplifying the design of the feedback and feedforward controllers. Because you cannot realize a design-model inverse, you must add a unity-gain lowpass filter specifying the observer bandwidth.

Next, the feedback controller forces dynamic consistency by mitigating the effects of model uncertainty and disturbances, usually with high gain and integral control. Engineers commonly make the mistake of designing the feedback controller for desired output with no regard for robustness, only to find poor performance when they apply the controller to the physical system. However, once you enforce consistency, you can augment the desired output with a feedforward controller, typically the dynamic model's inverse, to recover the dynamic delay of the closed-loop system. This approach has no effect on stability or the properties of the closed-loop system.

The combination of a disturbance observer with both feedback and feedforward controllers is not new, and many researchers have demonstrated its effectiveness. They now need to bridge that theory/practice gap and put this technique into the hands of the mechatronics engineers responsible for creating the innovative systems we all need. EDN

Kevin C Craig, PhD, is the Robert C Greenheck chair in engineering design and a professor of mechanical engineering, College of Engineering, Marquette University.

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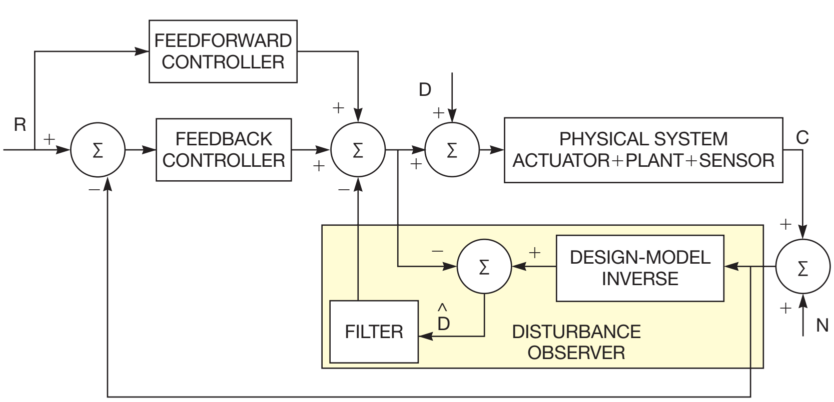

Figure 1 An integrated control system can enhance a design through stabilization, command following, disturbance and noise rejection, and robustness.

BY GINA BONINI • TEKTRONIX

Understanding SYSTEM-LEVEL ENERGY-MANAGEMENT techniques and test

REVIEW TEST EXAMPLES OF SYSTEM-LEVEL ENERGY-MANAGEMENT DESIGN TECHNIQUES FOR PCIe AND LOW-POWER DDR MEMORY.

Energy-management techniques, such as dynamic-power management, dynamic voltage scaling, and dynamic frequency scaling, have emerged as effective ways to reduce power consumption—a critical requirement in today's embedded-system designs. However, these techniques increase the complexity of test for design validation and debug. These schemes reduce power consumption by shutting down idle components or reducing the performance of components to provide just enough performance for a task. These techniques work on both processing elements, such as CPUs, FPGAs, and ASICs, and the communication buses that transfer data between these elements.

POWER DISSIPATION

Static-power dissipation occurs when you turn on a processing element, and dynamic-power dissipation occurs during computations. You can represent the total power dissipation as the sum of the static power and the dynamic power. The static-power dissipation occurs even when no computations are occurring. Leakage power and bias power are the main contributors to static-power usage.

Dynamic-power dissipation results from short-circuit power and switching power. The short-circuit power consumption is proportional to the supply voltage. The switching power dissipates when the parasitic capacitors of the transistor gates charge and discharge during computational tasks. So the processing element's power usage is equal to the sum of leakage power, bias power, short-circuit power, and switching power, where leakage power and bias power contribute to static power, and short-circuit and switching power contribute to dynamic power.

The switching power is the dominant source of power usage, accounting for approximately 90% of the total power that mainstream processing elements consume (**Reference 1**). The common **equation** for calculating the switching power of a processing element is:

$$P_{SW}=\alpha\times C_L\times V_{DD}^2\times F,$$

where P_{SW} is the switching power; α is a constant representing the switching activity for the computational task; C_L is the effective circuit-load capacitance, which you can assume to be a constant that the complexity of the design and the circuit technology determines; V_{DD} is the supply voltage; and F is the clock frequency (**Reference 2**).

This **equation** shows that you can reduce either the processing element's frequency of operation or the supply voltage to reduce switching-power dissipation. Because switching power is proportional to the supply voltage squared,

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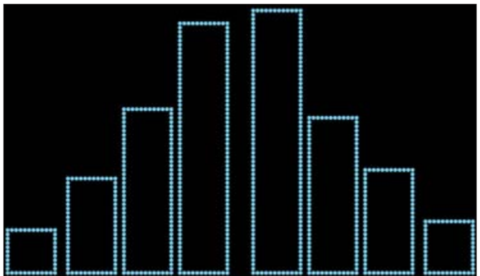

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you can achieve the largest energy savings by reducing the circuit's supply voltage. In some cases, you can achieve further energy savings by also reducing the operation frequency. You must carefully apply this technique because it increases processing time. Because power dissipation over time determines energy dissipation, you may achieve no energy savings if extra processing time is necessary. However, careful application of both frequency and voltage scaling offers higher energy savings than voltage scaling alone. Reducing supply voltage also reduces leakage-power consumption, improving static-power dissipation (**Reference 3**).

Dynamic-power management uses standby or sleep modes to reduce power consumption. Because it takes time and energy to reactivate processing elements and buses, you should carefully apply dynamic-power management to ensure that no violations occur in the system's operation or, in the worst case, no increases in power consumption from reactivation occur. Components still dissipate energy in standby as static power determines.

Dynamic voltage and frequency scaling reduces switching-power dissipation. This process can increase computation time, so you can apply dynamic frequency scaling only when there is slack time in the system-level operation of the design. **Figure 1** shows an example of dynamic voltage and frequency scaling. In this case, the system schedule allows 30 msec for Processing Element 2 to complete a task. However, the processing element completes the task in 15 msec, leaving 15 msec of slack time. The supply voltage and operational frequency of this element decrease until the task completes in 30 msec to match the system's schedule. Doing so decreases Processing Element 2's power consumption.

AT A GLANCE

- Dynamic-power management, dynamic voltage scaling, and dynamic frequency scaling have emerged as effective ways to reduce power consumption.
- Leakage power and bias power are the main contributors to static-power usage.
- Communication between elements is essential in embedded systems with multiple processing elements.
- PCIe (PCI Express) specifications allow for active-state power management, which conserves power by putting the bus into a power-saving state or dynamically configuring the link's width or speed.

You can also use dynamic-power management to maximize a design's energy efficiency. Even if you apply dynamic voltage and frequency scaling to all components that are adapting their performance to the requirements of the system schedule and minimizing energy consumption, idle times may still occur. You can then use dynamic-power management to shut down components that are idle for a time for even further energy savings.

BUS ENERGY DISSIPATION

Communication between elements is essential in embedded systems with multiple processing elements. With every data transfer over a communications bus, the line capacitance charges and discharges, drawing current from the I/O pins of the elements. The following **equation** calculates the power that these currents dissipate:

$$P_{CL}=\beta\times C_{BUS}\times F_{BUS}\times V_{TR}^{2},$$

where P_{CL} is the power loss that these currents dissipate, $\beta\times C_{BUS}$ represents the switched load capacitance of the bus, F_{BUS} is the operational frequency of the bus, and V_{TR} is the transmission voltage.

You can reduce the transmission voltage in communications buses only to a limit because of noise issues. Noise can more easily corrupt low-voltage communications, causing reliability problems. As with dynamic frequency scaling, you can scale down the operational frequency or data-transfer rate of the bus if the system schedule has slack time for bus communication. You can also put the bus into a standby state during idle times in an approach similar to dynamic-power management.

Low-power DDR (double-data-rate) DRAM devices and several popular communication buses offer low-power modes. These buses include PCIe (PCI Express), MIPI D-PHY and M-PHY, USB 3.0, and MXM (Mobile PCIe Module). Debugging these buses presents a number of challenges.

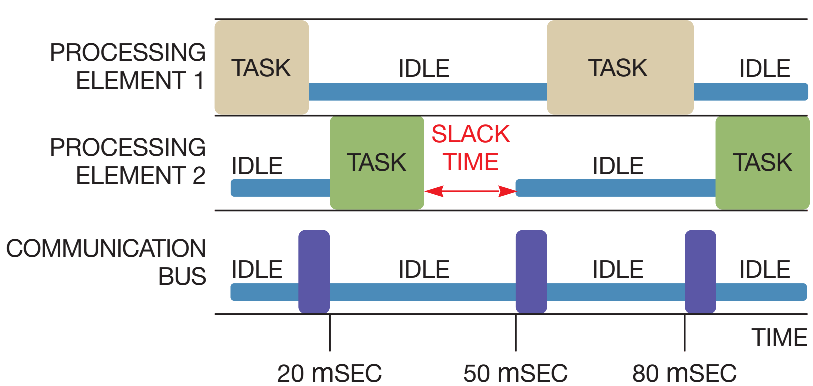


Figure 1 In dynamic voltage and frequency scaling, the system's schedule allows for 30 msec for Processing Element 2 to complete a task.

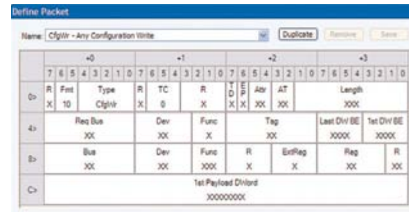


Figure 2 A logic analyzer with a serial module for PCIe is the troubleshooting tool of choice because it allows you to trigger on a transaction-layer-packet-configuration write based on the bus, device, and function number.

PCIe'S LOW-POWER MODE

PCIe specifications provide active-state power management that conserves power by putting the bus into a power-saving state or dynamically configuring the link's width or speed. Validation and verification of a PCIe bus are complicated because of these features. Problems can arise when the system enters or exits one of the power-saving link states or when the link's width or speed changes dynamically in response to system requirements.

Table 1 (pg 36) lists the PCIe's link power states. To maintain synchronization between the transmitter and the receiver, the bus must transmit idle symbols over the link when there is no data available. The receiver decodes and discards these idle symbols. To save power during these periods, you can put the link into a power-saving state. The power savings and the time to recover back to the L_0 state increase as the link moves from the L_0 state to the L_3 state.

To understand how this situation increases complexity, consider a case in which a PCIe link is in the L_0 state and moves to the L_{0S} state. Immediately after the transition, a transaction-layer-packet configuration write occurs that writes an incorrect value to a register, causing the system to crash. To troubleshoot this problem, you must acquire all the transactions that occur during the transition from the L_{0S} state to the L_0 state.

In such a case, a logic analyzer with a serial module for PCIe would be the troubleshooting tool of choice because it allows you to trigger on an event. For example, in this scenario, the logic analyzer would trigger on a transaction-layer-packet configuration write based on the bus, device, and function number (**Figure 2**).

After you define the trigger, the serial module can bit-lock and align the data across all the lanes of the bus after observing approximately 12 fast-training-sequence packets as the link exits the L_{0S} state and enters the L_0 state. Because the logic analyzer can track the change in the link state, it can acquire all transactions that occur immediately after the bus enters the L_0 state, providing insight into the cause of the system crash.

To save memory, you can also set up the logic analyzer to filter out unwant-

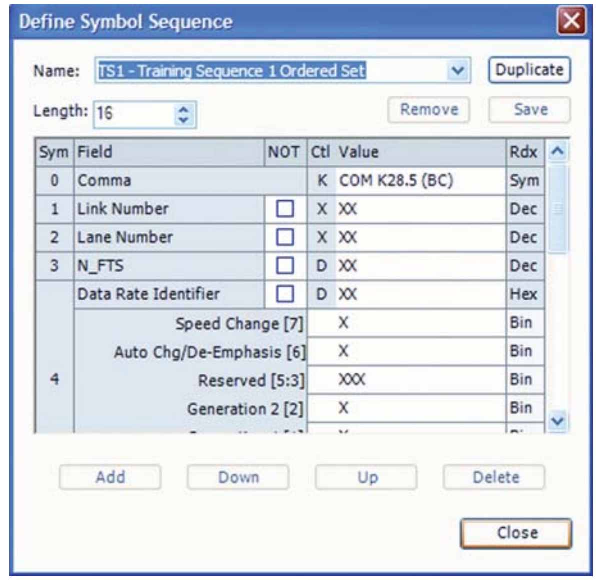


Figure 3 You use this type of dialogue to set up the condition for triggering on a training sequence.

ed data in real time, focusing data acquisition on problem areas. A common use of filtering occurs when the PCIe bus is in the idle state. You can define a filter to filter the idle symbols in real time, storing only the required data and thus making more efficient use of the logic analyzer's memory and capturing more relevant data that helps in troubleshooting the problem.

The PCIe specification also provides for dynamically changing the link's width or speed depending on the need to conserve power or provide performance. These dynamic changes in the link's condition can be challenging to debug.

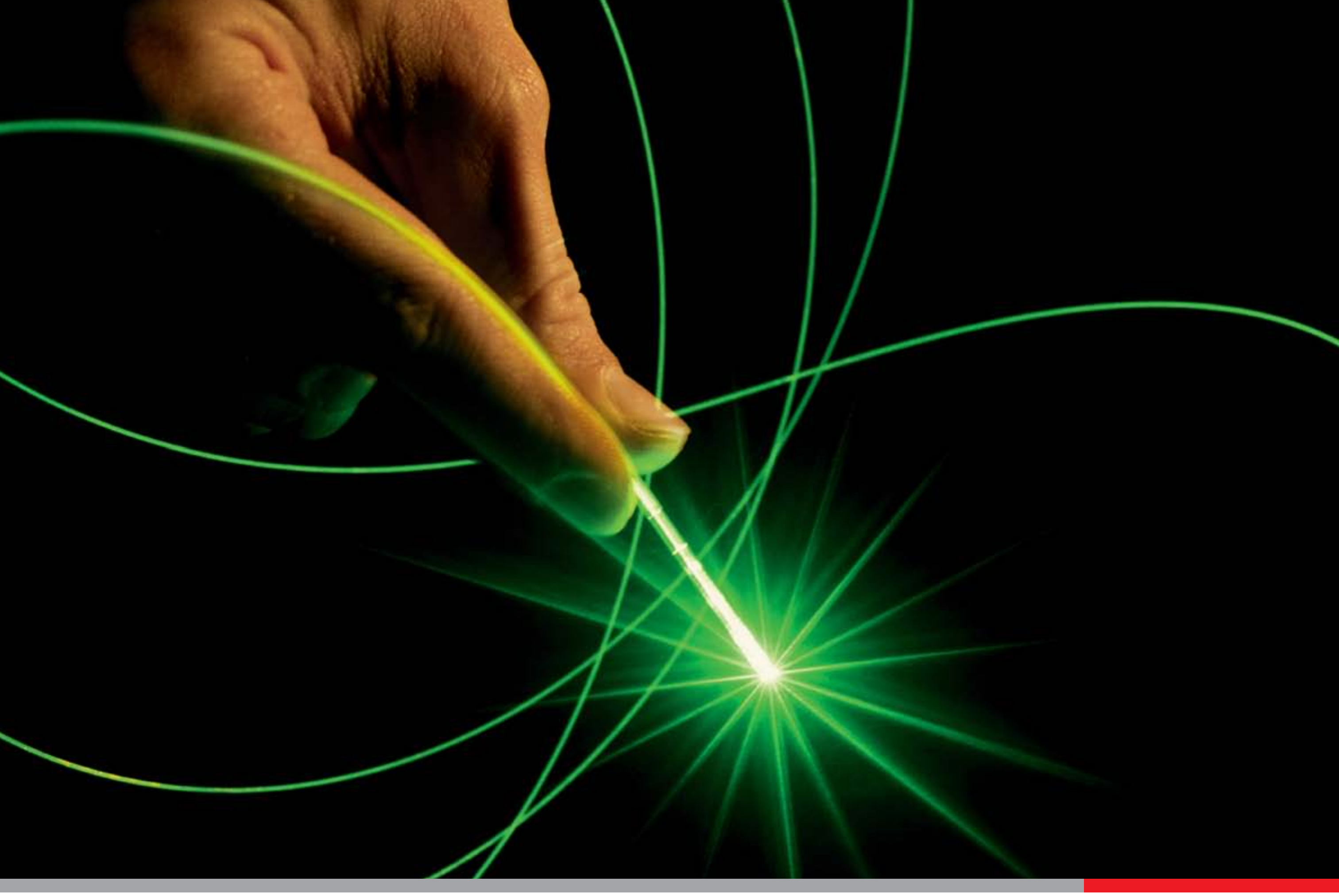
Consider a case in which the link's width is changing from eight lanes to four lanes. Here, you can use a logic analyzer to trigger on and acquire the training sequences that occur during the link-speed change and the link-width negotiation process, allowing you to validate that the link is training to the correct width. **Figure 3** shows the type of dialogue you use to set up the condition for triggering on a training sequence. In some cases, due to errors in the link, you may not find the required trigger conditions. In such instances, you may need to build a customized sequence and set it as a trigger condition on a lane. This approach is faster than manually looking through the data to figure out the problems in the link. To identify errors in the physical layer, logical analyzers offer link-event triggers. For this trigger, the event could be disparity, an 8/10b error, or an error in framing the data-link-layer or the transaction-layer packets.

LOW-POWER DDR MEMORY, OR MOBILE DDR, OPERATES AT 1.8V RATHER THAN THE MORE TRADITIONAL 2.5V.

LOW-POWER DDR MEMORY

Low-power DDR memory, or mobile DDR, helps reduce energy requirements by providing more efficient device operation. It operates at 1.8V rather than the more traditional 2.5V. Low-power DDR DRAM commonly finds use in portable electronic devices, and line-powered electronics are increasingly adopting it as a way to reduce energy requirements.

Reducing operating voltage is a trend that extends beyond low-power DDR memory to more mainstream memory technologies, as well. DDR2, which originally operated at 2.5V, has seen later variants that lower the requirement to 1.8V, and further reductions are in development. Similarly, DDR3 once operated at a supply voltage of 1.5V but will soon see that figure decrease to 1.35V for some new components. Low-power DDR2, the newest entry in this power-



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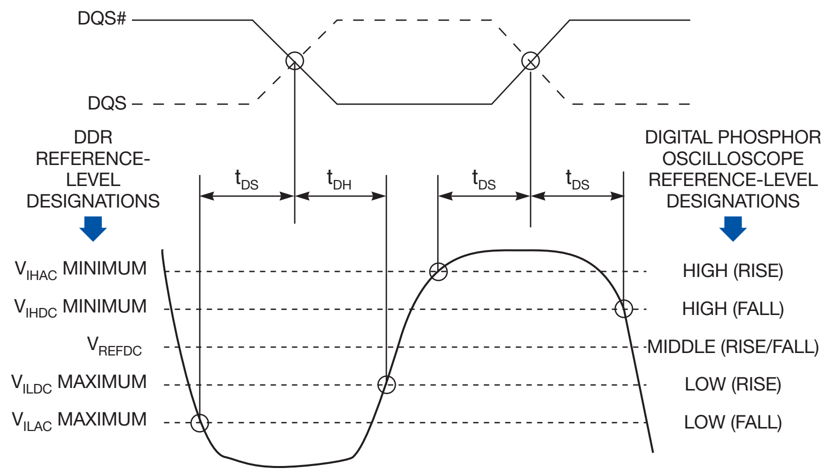

Figure 4 Timing measurements on data signals use both the ac and the dc high and low input-voltage levels.

reduction trend, requires only 1.2V.

You can achieve additional energy savings by reducing the performance of the device. Low-power DDR and other DDR standards specify power-saving modes of operation that reduce performance depending on the system's needs.

POWER-SAVING MODES

Because DRAM cells leak off charge, they must regularly refresh their contents during modes of operation requiring maintenance of data. The low-power-DDR-DRAM specification calls for three refresh modes to minimize power dissipation and maintain the required data states. The most basic mode, self-refresh, generates a low-frequency internal clock to maintain the contents of the DRAM. Temperature-compensated self-refresh automatically modifies the internal refresh clock frequency depending on the temperature of the low-power DDR DRAM. During lower operating temperatures, the refresh time can be longer to save power. Partial-array self-refresh maintains data in only a portion of the DRAM.

When the low-power-DDR-DRAM device does not need to retain data and when access to the DRAM is not necessary for several seconds, the device can use the power-down mode.

A system's power consumption is proportional to the frequency at which the clock is changing. The low-power-DDR-memory standard stipulates many power-saving modes that leverage the frequency component of this power equation. The power-saving refresh modes reduce the clock frequency to reduce power consumption. The power-down mode can put the DRAM into standby mode during inactive periods. All of these power-saving modes primarily affect static-power consumption.

You can reduce dynamic-power consumption by optimizing data throughput, allowing the operating frequency of the device to decrease and still meet performance requirements. The ability to do this task is a key differentiator of low-power-DDR-DRAM devices.

LOW-POWER DDR DRAM

JEDEC (Joint Electron Device Engineering Committee) has specified the jitter, timing, and electrical-signal-quality tests for validating memory devices. The JEDEC specifications describe a comprehensive set of tests for each memory technology, including parameters such as clock jitter, setup-and-hold timing, signal overshoot, undershoot, and transition voltages. These specified tests are not only numerous but also complex to measure using general-purpose tools.

An example is measurement reference levels. JEDEC specifies certain voltage reference levels that you must use when making timing measurements. **Figure 4** shows the ac and dc high and low input-voltage levels that timing measurements on data signals use. JEDEC defines the levels for rising and falling edges differently. Because of the complexity inherent in the JEDEC-specified measurement methods, including reference levels and pass/fail limits, the preferred approach is to use an application-specific measure-

Figure 5 To ease setup tasks, a menu-driven interface guides you through a selection process.

Figure 6 The menu groups available measurements according to which signals and probing connections are necessary.

TABLE 1 PCIe LINK STATES

L_0: active state	All transactions are enabled, and link is operating in normal mode
L_{0S}: low resume latency, energy-saving standby	
L_1: higher latency, low-power standby	All power supplies and reference clocks are active, transaction-layer-packet and data-link-layer packet transmission are disabled
L_2/L_3: staging point for transition to L_2 or L_3	Transaction-layer-packet and data-link-layer packet transmission are disabled
L_2: auxiliary powered link, deep energy-saving	Main power supply and reference clocks are off
L_3: link off	Link is in this state when no power is applied

ment utility for DDR test. Using such a utility ensures that you configure measurements according to the specification and reduces setup time.

With real-time-performance oscilloscopes, DDR software utilities provide a broad set of measurements that conform to the JEDEC specifications. In addition, these utilities allow you to customize many settings to accommodate measurement tasks on nonstandard devices or system implementations and to aid in debugging. To ease setup tasks, a menu-driven interface guides the user through a selection process (**Figure 5**).

The first step of such an interface is to select the DDR generation you want to test and the speed grade of the memory. In addition to the default choices, the use of custom speed settings makes the software adaptable to future technology advances, overclocking applications, and the like. Once you have selected the generation and data rate, the software configures the correct voltage references for measurements. The next step is to select which measurements to perform (**Figure 6**). The menu groups available measurements according to which signals and probing connections are necessary. The remaining steps guide you on how to probe the needed signals and offer additional opportunities for customizing or adjusting parameters, such as measurement reference levels.

Once the setup is complete, the oscilloscope acquires the signals of interest, identifies and marks data bursts if needed, and makes the selected measurements. A results panel shows all measurement results with statistical population, spec limits, pass/fail results, and other data (**Figure 7**). You can at this point print a report, with an option to also save the waveform data that you used to make the measurements.

Because the captured waveform data is available with the measurement results, you can use this information for further analysis. For example, if a measurement fails the spec limits, you can identify exactly where in the waveform record the failure occurred and then zoom in on the region of interest to investigate the exact signal details and characteristics at the time of failure.

System-level energy-management techniques look at the system-level operation of a design for opportunities to lower power consumption by shutting down components or scaling voltage and frequency. Test-and-measurement tools have evolved to help designers debug systems in the face of this increased complexity.

For instance, logic analyzers offer trigger capability with a layout similar to the definitions in the standard they are testing—a helpful technique in finding elusive problems resulting from active-state management. Similarly, validating DDR-DRAM devices requires performing the numerous tests in the JEDEC specifications, a time-consuming and complicated task. By using specialized software together with a high-performance real-time oscilloscope, you can access a broad set of automated measurements, simplifying the validation of memory devices. **EDN**

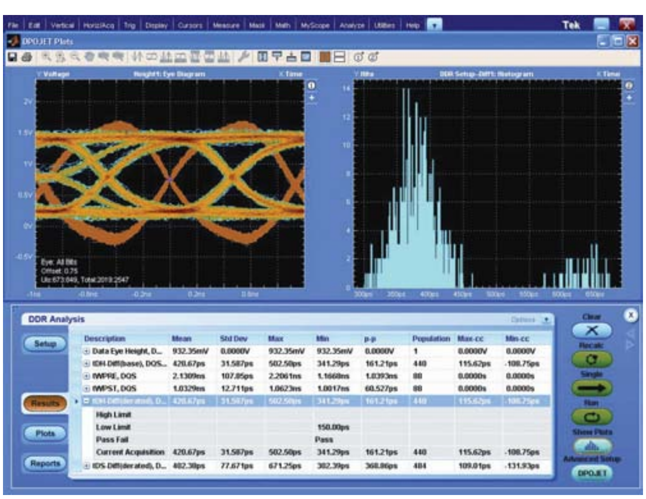

Figure 7 A results panel shows all measurement results with statistical population, spec limits, pass/fail data, and other data.

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AUTHOR'S BIOGRAPHY

Gina Bonini is the worldwide embedded-system technical-marketing manager for Tektronix. She has for more than 15 years worked extensively in various test-and-measurement positions, including product planning, product marketing, and business and market development. She holds a bachelor's degree in chemical engineering from the University of California—Berkeley and a master's degree in electrical engineering from Stanford University (Stanford, CA).

VOLTAGE REFERENCES HOLD STEADY

THESE UBIQUITOUS PARTS KEEP GETTING BETTER, AND SELECTING THEM INVOLVES CAREFULLY WEIGHING MANY SPECS AND TRADE-OFFS.

BY PAUL RAKO • TECHNICAL EDITOR

Voltage references are low-output-power linear supply regulators that produce a fixed, or constant, voltage regardless of the loading on the device, power-supply variations, temperature changes, and the passage of time. As a result, voltage references are ubiquitous in power-supply voltage regulators, data-acquisition systems, ADCs, DACs, and myriad other measurement-and-control systems. Despite their ubiquity, voltage references vary widely in performance. A regulator for a computer power supply, for example, may hold its value to only within a few percentage points of the nominal value, whereas laboratory voltage standards have precision and stability measurements in parts per million.

Decades ago, these references provided initial accuracies of only ±10%, whereas modern reference ICs can provide initial accuracies of 100 ppm, or 0.01%. "We try to make the parts insensitive to line, load, and temperature variations for demanding tasks in the industrial, scientific, and medical markets," notes Reza Moghimi, application-engineering manager at Analog Devices. Companies with expertise in those markets can also easily address the military and automotive markets, in which accuracy is critical.

Voltage-regulator chips are available in series and shunt versions (**Figure 1** and **Reference 1**). A series regulator has two pins for input power and ground; a third pin outputs a fixed or adjustable voltage. Two-terminal shunt regulators operate at a current-limited, fixed voltage. In essence, every voltage regulator employs a shunt architecture because a series reference is simply a shunt reference with a current-feeding circuit and a buffered output.

In the early days of electronics, engineers used neon glow tubes as voltage references (**Figure 2**). The neon glow lamp comprises two conductive terminals in a glass container filled with rare, or noble, gases—chemical elements with similar properties. Under standard conditions, they are all odorless, colorless, monatomic gases, with low chemical reactivity. The six noble gases that occur naturally are helium, neon, argon, krypton, xenon, and radon. The gases ionize when you subject them to a voltage of 66 to 200V dc. Once the ionized breakdown occurs, the voltage across the lamp drops to a maintenance voltage of 48 to 80V dc. If the voltage across the lamps drops below this maintenance voltage, the lamp goes out, and you must again subject it to the ionizing breakdown voltage to get it to light (**Figure 3**). A neon glow tube works on as little as 10^{-12}A, or 1 pA, flowing through it. In 1966, Signalite made tubes that could provide regulation to within ±0.5V (**Reference 2**).

By the 1970s, however, zener diodes, which are shunt references, had obsoleted these cold-cathode glow tubes (**Figure 4**). Zener diodes take their name from researcher Clarence Zener, who discovered the effect (**Reference 3**). Although some engineers refer to zener diodes as avalanche diodes, the two types involve different physics (**references 4**, **5**, and **6**). Zener breakdown results from charge carriers that perform quantum mechanical tunneling through a PN junction. This breakdown occurs in heavily doped junctions. High electric fields in the PN junction accelerate charge carriers, causing avalanche breakdown. These speedy carriers cause impact ionization, which in turn causes charge carriers to multiply. This effect occurs in lightly doped PN junctions. Zener-diode manufacturers take advantage of these two effects by varying the doping in the PN junction to create diodes with different breakdown voltages. The zener effect predominates in diodes with voltages as high as 5.6V, and the avalanche effect predominates at higher voltages. The two effects also differ in their temperature coefficients: Zener devices have negative breakdowns, whereas avalanche devices have positive breakdowns. Diodes that break down at 5.6V combine the two effects and have a small temperature coefficient because the positive and negative coefficients cancel out.

AT A GLANCE

- Voltage references can operate as series or shunt elements.
- Primitive references include neon tubes and discrete zener diodes.
- IC references can employ buried zener diodes, bandgaps, JFETs, or floating-gate architectures.
- Many specifications are important for references.
- Be sure to look at the system implications of your reference's accuracy.

LIKE BURIED JFETs, BURIED ZENER DIODES DO NOT TOUCH SURFACE DEFECTS IN THE DIE, MEANING THAT THE DIODES OPERATE AT LOW NOISE LEVELS.

As ICs became popular in the 1970s, it became essential that they integrate a shunt voltage reference. Companies such as Burr Brown, Analog Devices, and National Semiconductor then used the approach of burying zener diodes in their ICs (**Figure 5**). The IC-process steps create the device under the surface layer of the die. Like buried JFETs, buried zener diodes do not touch surface defects in the die, meaning that the diodes operate at low noise levels.

In 1971, US electronics engineer Bob Widlar, a pioneer of linear-analog-IC design, employed a voltage reference that he based on the bandgap-voltage effect that the late DF Hilbiber, then an engineer at Fairchild Semiconductor, discovered in 1964. The bandgap reference has an inherent 1.2V output voltage, approximately the bandgap voltage of silicon at 0°K (**Figure 6**). Devices with other output voltages simply increase or decrease the voltage with internal gain circuits. Analog-IC designer Bob Pease improved on Widlar's designs and helped IC designers at National Semiconductor use the bandgap circuit in dozens of chips (**Reference 7**). "In the 1980s, 40 to 60% of the bandgap [voltage-effect references] we brought out had old, dumb errors," Pease remarks. "Many such errors are related to IC layout, and we fixed them with a good design review."

In 1974, Paul Brokaw, now senior technologist at Integrated Device Technology, designed a bandgap voltage that used feedback to improve accuracy and

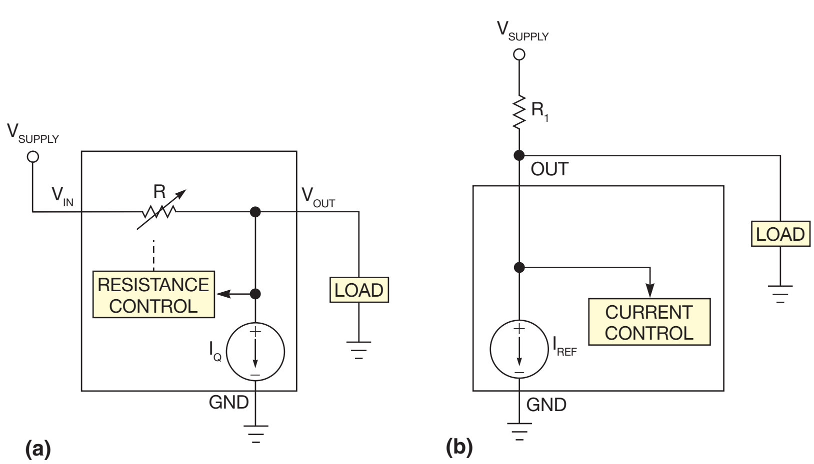

Figure 1 A series reference has three terminals (a). Some ICs buffer the output with an internal op amp. A shunt reference is a two-terminal device (b) (courtesy Maxim Integrated Products).

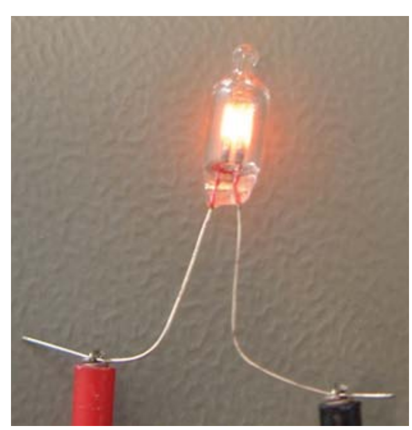

Figure 2 Neon lamps served as references before IC-semiconductor engineers designed solid-state voltage regulators in the 1960s (courtesy www.giangrandi.ch).

reduce errors (**Figure 7**). "I dreamed it up when trying to make a discrete power supply, and I wanted to use a lower reference voltage than a 6.8V zener diode," says Brokaw.

In addition to the buried-zener and bandgap-type voltage references, JFET-based devices, such as the Analog Devices' ADR440, are also available (**Figure 8**). The buried JFETs help these parts achieve noise specs of 1 μV p-p over 0.1 to 10 Hz. Analog Devices' Moghimi also alludes to a new class of references that the company will introduce this year that employs a different architecture from any of the techniques this article describes.

SOME REFERENCES EMPLOY FLOATING-GATE FETs SIMILAR TO THE STRUCTURES THAT FLASH MEMORY USES BUT EMPLOYING AN ANALOG VOLTAGE.

Other references, such as those from Intersil, employ floating-gate FETs similar to the structures that flash memory uses but programmed to an analog voltage (**Reference 8** and **Figure 9**). Intersil buffers the voltage within the device, so no leakage currents come from ESD (electrostatic-discharge) diodes that would bleed off the charge on the floating gate. These parts use little cur-

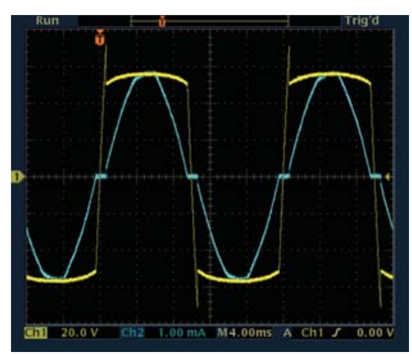

Figure 3 The voltage across a neon lamp (yellow) can rise to a high value until the gas in the lamp ionizes. Once the gas ionizes and the lamp conducts, the voltage drops and stays relatively constant despite the ac current flowing in the lamp (blue) (courtesy www.giangrandi.ch).


MEET THE GUY that ELIMINATED HIS TEAM'S
MANUFACTURING VARIABILITY ISSUES.

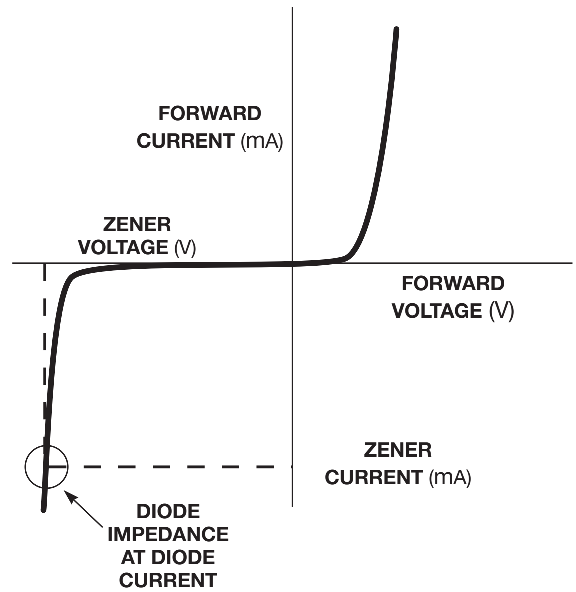

Figure 4 A zener diode acts as a conventional diode in the upper right quadrant of this voltage-versus-current plot. In the lower left, the voltage breaks down, and voltage is relatively constant across the device (courtesy Renesas).

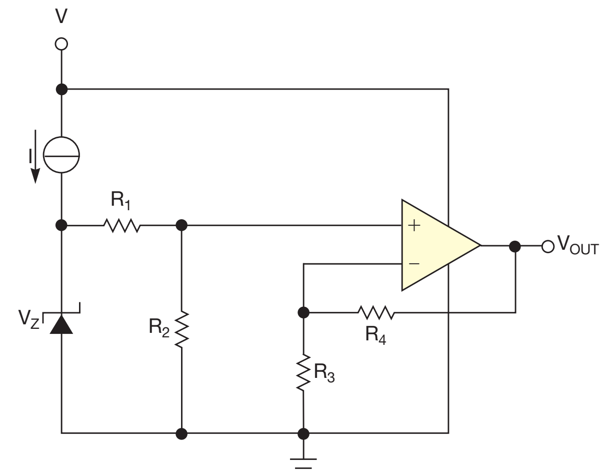

Figure 5 A buried-zener reference IC takes advantage of the low noise of a device under the surface layer of the die (courtesy Texas Instruments).

rent but have better noise performance than low-power voltage references using conventional architectures. Barry Harvey, IC-design manager at Intersil, notes that the references required some clever tricks in both the process and the IC design. "Once we perfected it, we found that leakage off the floating gate was in the range of attoamps, [10^{-18}A], even at high temperatures," he says. By using a floating gate instead of a bandgap, Intersil can program one die to make parts offering dozens of output voltages.

VOLTAGE-REFERENCE SPECS

Voltage references have two fundamental specs: load regulation and line regulation. Load regulation relates to the change in the output as the part draws more current. Line regulation refers to the change in output as the power supplying the part changes. Transient regulation, or output impedance, also relates to load regulation. Output voltage must stay in range even if your system draws sudden current pulses from the reference IC. Some modern ADCs have reference inputs that draw large transients from your part. You can sometimes fix this problem by adding a large-output filtering capacitor, but you must be careful that you don't cause the reference to become unstable.

You must understand several specifications to properly select and apply voltage references. You need not worry about the internal architecture. It is more important to know the specifications of the part, not how the IC company designs it internally. Besides deciding between shunt and series regulators, you must determine whether a zener diode would work in your system. In most cases, you are better off using a specialized voltage-reference IC from an analog-chip company. If you need ultralow power, you should use a series voltage reference, such as a floating-gate device from Intersil. Linear Technology offers the bipolar LT6656, which operates from less than 1 μA of supply current.

After you consider your power budget and select a series or a shunt reference and an output voltage, you must consider the device's initial accuracy—that is, the accuracy at room temperature when you first apply power to the part. Some adjustable references let you set the output voltage or shunt voltage with one or two resistors. The accuracy of those resistors combines with the stated initial accuracy of the chip to give you a total initial accuracy of your output voltage. More commonly, you select a part with a fixed voltage output of 1.2 to 12V. The initial accuracy of the device determines how closely all the parts you buy approach that ideal voltage output. Using discrete zener diodes or older legacy references, you can expect to achieve 10% accuracy, meaning that you must calibrate or adjust the circuits in production. Modern parts, such as Analog Devices' AD588, have initial accuracies approaching 0.01%. This spec is critical in data-acquisition systems that require accuracies of

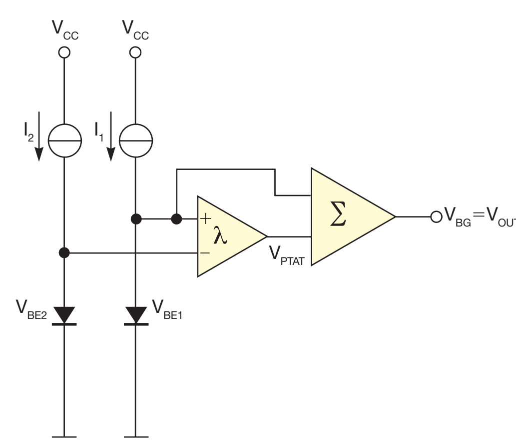

Figure 6 In a bandgap reference, the temperature coefficients of the V_{BE} (base-to-emitter voltage) and the difference, or delta, between two base-to-emitter voltages cancel out. The difference, V_{PTAT}, is the voltage proportional to absolute temperature on the Kelvin scale (courtesy Texas Instruments).

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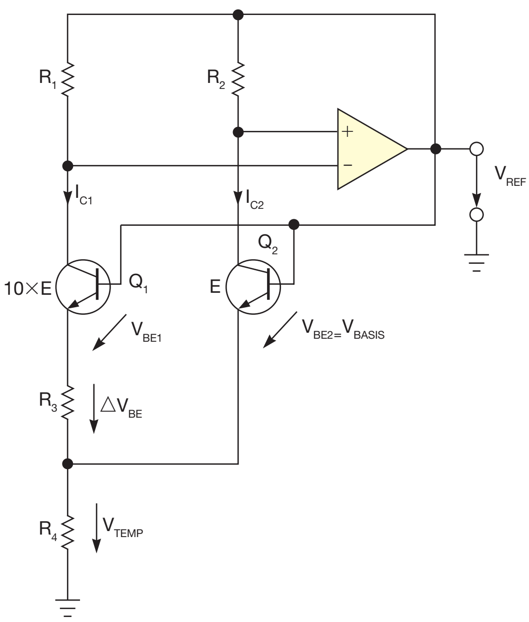

Figure 7 The Brokaw cell uses feedback to reduce the error terms of a Widlar-style bandgap circuit.

16, 18, or even 20 bits. Another factor driving the adoption of parts with high initial accuracy is the requirement for charging lithium-ion batteries. The design of charger ICs or the process of measuring the charging voltage of a lithium-ion battery requires a total accuracy better than 0.5%. Thus, the voltage reference should have initial accuracies close to 0.2% to keep total system inaccuracy to less than the 0.5% figure that battery-cell manufacturers specify.

Once you have specified the initial accuracy, you can begin to consider output-voltage drift. Temperature drift, which designers often express as a temperature coefficient in parts per million per degree Celsius, reveals how much the IC's output voltage changes as the ambient temperature changes. If you specify your system over a large temperature range, such as automotive or military circuits, you have to look at the accuracy of the device across the entire temperature range and add that accuracy to the initial accuracy of the part.

Once you have specified the initial accuracy and temperature drift of the part, you then have to look at the stability, or output-voltage drift, over time. Most parts change over the first six months of operation and then settle down to a smaller change over time. Again, the output drift adds to the initial inaccuracy and temperature drift. If

FIRMWARE ENGINEERS SHOULD NOT MAKE READINGS OR DO CALIBRATION IN THE FIRST FEW MICROSECONDS OF A CIRCUIT'S OPERATION.

you want your system to have a tight accuracy over its operating life, you must use parts that have a long-term drift speciation that keeps your system's reference voltage within the desired limits. You can also average the output of multiple parts to reduce the effect of output drift over time (**Reference 9**). Some manufacturers take the extra steps of determining, specifying, and measuring temperature drift and long-term stability of a part, and these steps take time and come at a price. For example, Analog Devices tests the ADR425 voltage reference for a long-term stability of 50 ppm/1000 hours.

A related but less appreciated specification is the turn-on settling time of a reference IC. The output of an IC does not instantly stay within specified limits, so firmware engineers should not make readings or do calibration in the first few microseconds of a circuit's operation. Many parts specify a 10-µsec delay after you apply power to the part.

Another important specification is noise. Because series references are simply op-amp-buffered shunt references, you can expect the output to have noise characteristics similar to those of an op amp. The noise spectrum is flatband at higher frequencies. Because you use voltage references for their dc output, however, most manufacturers specify their products with a peak-to-peak output-noise voltage over a frequency

TABLE 1 VOLTAGE-REFERENCE SPECS

Parameter	Cirrus Logic VRE3050	Maxim MAX6250	Analog Devices ADR293
Temperature range (°C)	–40 to +85	–40 to +85	–40 to +85
Output voltage (V)	5	5	5
Initial error (%)	0.01	0.05	0.06
Temperature coefficient (ppm/°C)	0.6	3	8
Noise at 0.1 to 10 Hz (µV p-p)	3	3	15
Thermal hysteresis at 25 to 50 to 25°C (ppm)	2	20	15
Long-term stability (ppm/1000 hours)	6	20	0.2
Power supply (V)	8 to 36	8 to 36	6 to 15
Turn-on settling time (µsec)	10	10	10
Line regulation at 8V≤V_{IN}≤ 10V (ppm/V)	25	35	100
Load regulation at a source of 0 mA≤I_O15 mA (ppm/mA)	5	7	100
Power-supply-rejection ratio at 10 to 900 Hz (dB)	95	90	40

Source: Texas Instruments

range of 0.1 to 10 Hz, for example. You might be able to reduce this noise by increasing the output capacitance, but you must be careful to not make the reference unstable. As with all op-amp circuits, driving a large capacitive load makes the amplifier oscillate. Analog Devices' Moghimi wishes that analog designers would more carefully read modern reference data sheets. "Some customers still think it is good to put a large output capacitor on the part," he says. "Even if it does not cause stability problems, it can cause the temperature coefficient to get much worse."

Another trick for reducing noise is to parallel several voltage references and add the outputs together. Noise is a random phenomenon, so the noise contribution of each reference adds in an rms (root/mean/square) fashion. Thus, 10 paralleled references can potentially reduce the voltage noise by the square root of 10, or over a factor of three (**Figure 10**). State-of-the-art references, such as Linear Technology's LTC6655, have a noise spec of 0.625 µV p-p over 0.1 to 10 Hz.

Still another specification, which relates to the temperature coefficient, is hysteresis—an effect in which the output drifts to another level when you heat the part and then cool it down to its original temperature. Manufacturers often specify it as a part-per-million value over a temperature traversal such as 0 to 50 to 0°C. Like all other analog circuits, voltage-references chips also have a PSRR (power-supply-rejection ratio)—how much attenuation the part applies to any noise or changes in the power supply that is feeding the part. This spec is important now that more systems use switching voltage regulators to supply the reference IC. Manufacturers often specify this characteristic as a voltage ratio in decibels at dc or over a frequency range. PSRR always drops off at higher frequencies, often falling to 20 dB or less at 1 MHz. If your voltage-reference chip is operating from a power supply comprising a switching regulator operating at these high frequencies, you must ensure that the ripple and noise on the power supply do not bleed into the reference-voltage output due to poor high-frequency PSRR. You can often fix these problems by putting a linear preregulator IC on the switching-power-supply output that feeds your reference chip. You can also put RC (resistance/capacitance) or RLC (resistance/inductance/capacitance) filters

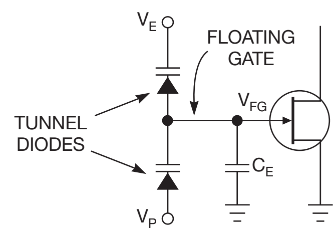

Figure 9 Intersil used floating-gate technology from its acquisition of Xicor to create a line of voltage references that use low power and have low noise.

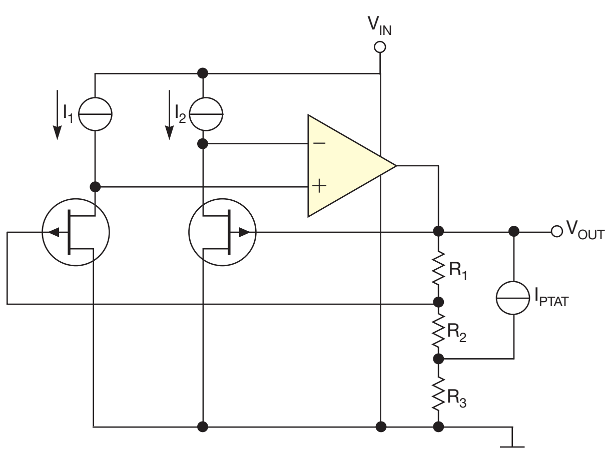

Figure 8 A JFE T-based voltage reference uses the difference between two JFET drain voltages to create a stable voltage. The I_{PTAT} source creates a current proportional to absolute temperature (courtesy Texas Instruments).

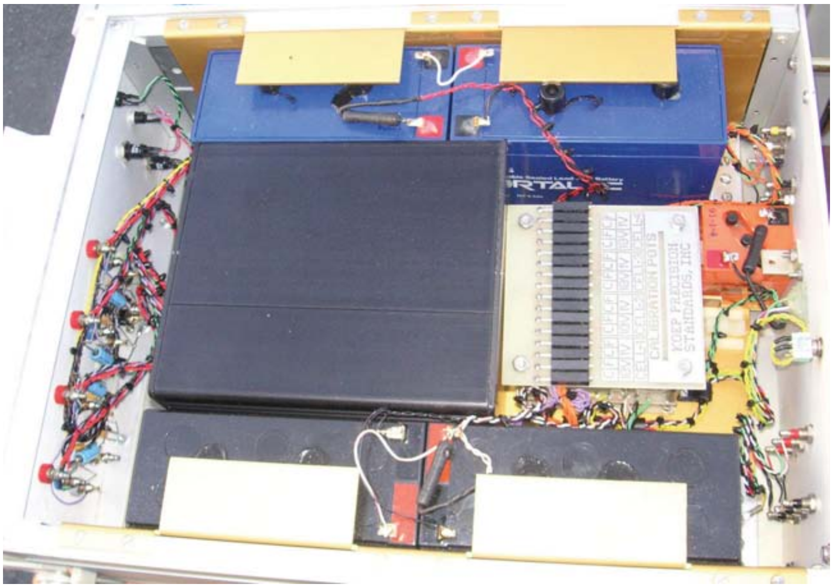

Figure 10 This four-cell voltage reference, which the late Kenneth Koep designed, uses batteries to keep the circuit operating when unplugged. The zener reference cells are in constant-temperature ovens, and you can average the four cells to reduce noise and improve accuracy.

before the power-supply pin of the reference IC. This approach prevents the occurrence of high-frequency noise in the reference voltage.

Some engineers use Spice models of voltage references; keep in mind, however, that these models have varying quality. Analog Devices, for example, puts the effects of most of the specs into the model. Other companies do not model references at all. Be sure that your model run takes into account all the specs that will affect your design. You may have to do a Monte Carlo Spice run to see the limits of accuracy, but at least you will know the limitations of the parts you are evaluating.

TRADE-OFFS ABOUND

The accuracy and noise of a voltage reference are important parts of the system-design trade-offs you make. For instance, LCD televisions are adopting Class D audio subsystems. Class D amplifiers are similar to switching regulators in that they are more efficient than conventional Class AB amplifiers. One trade-off with Class D amps, however, is that they have worse PSRR than do linear output stages. As a result, you must use either a higher-quality power supply or a more expensive Class D IC with feedback that corrects errors due to power-supply-voltage changes. This trade-off directly affects your choice of voltage reference. You might use a low-noise voltage reference in a power-supply circuit with low ripple and good regulation. You can then use a less expensive, open-loop Class D-amplifier circuit in your audio systems. On the other hand, it may be less costly to use a Class D-amplifier IC that has feedback and good PSRR so that you can use a less expensive power-supply circuit. This trade-off will change over the years and over the power and cost targets that you have for the TV. Using a more expensive voltage-reference circuit can save money in other subsystems or in factory calibration or testing when you manufacture the product in volume.

As with anything in analog design, applying a voltage reference is more complex than you might think. Even though it has only two or three pins, many specs affect its quality (**Table 1**). Be sure you understand all the specs and why they are important. If you have any doubt, consult the application-engineering departments of the reference- and data-converter-IC manufacturers. They will be glad to help you understand the intricacies of applying voltage-reference ICs. Remember that, in the analog world, an initial-accuracy spec is just the starting point. Actual accuracy depends on time, temperature, power-supply quality, and a host of other factors. Factor the specifications of the reference circuit into error budgets at the start of your design to ensure that no problems arise when the circuit enters volume manufacturing. Then, you can celebrate instead of rushing around doing ECOs (engineering change orders) to get your reference to behave properly. **EDN**

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Texas Instruments
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BY ANDRÉ MARAIS • SYMMETRICOM INC

IEEE 1588-2008 perspectives and opportunities

THE REVISED PRECISION TIME PROTOCOL PRESENTS OPPORTUNITIES AND SOME REAL-LIFE CHALLENGES.

The PTP (Precision Time Protocol), which the IEEE defined under 1588-2008, represents a step change in the distribution of time and frequency across WANs (wide-area networks). The telecommunications industry is, in parallel, evolving to packet-transport systems, isolating services and systems from their clock sources. As a result, the mobile sector, in particular, represents the first large-scale opportunity for IEEE 1588.

SYNCHRONIZATION DEFINED

The words you speak and the images you see are analog, but transporting these base signals on a large scale is impractical. To make the process manageable and scalable, you digitize the signals and transport them over synchronous networks. A common frequency digitizes and rebuilds an acceptable reproduction of the voice and video signals at the remote end, meaning that the frequency at the source must be the same as the frequency at the destination. The transport networks also need a stable frequency for capacity multiplexing, service encoding/decoding, and quality-of-service measurements.

Every location in the network must operate at the same frequency, or exhibit synchronization. TDM (time-division-multiplexed) networks transport frequency, and the local oscillators in all transport and switching devices can connect to a centralized primary reference clock with accuracy of 1×10^{-11} or better. Unfortunately, TDM networks do not seamlessly transport the frequency, and this issue affects the clock's quality as the clock passes through the network. Synchronization-supply units remove the jitter and wander that affect the instantaneous frequency stability.

The universal demand for broadband data, especially mobile broadband services, and the price that consumers are willing to pay have driven a change in transport technologies. IP (Internet Protocol)-based packet networks increase the bandwidth and reduce the cost per bit transported. L2/L3 (Layer 2/Layer 3) packet networks are associated with Carrier Ethernet and IP transport and are now in wide use because they meet the investment goals: increased bandwidth and reduced cost per delivered bit.

L2/L3 networks do not need synchronization to transport packets. By the same token, L2/L3 networks do not transport synchronization, isolating services and applications from their traditional frequency source, the transport clock. Delivering more bandwidth for less, therefore, comes at a price. Synchronization and quality of service are not natural to L2/L3 networks, and engineers must consciously implement them in the system.

Many services need synchronization, but wireless base stations today have the largest stake in frequency and time distribution. The frequency stability of the air interface between the cell tower and the handset supports handing off a call between adjacent base stations without interruption. Synchronization for base stations is therefore central to the quality of service an operator provides.

Table 1 lists the frequency and timing requirements for wireless standards. The air-interface stability must be 50 ppb (parts per billion), or 5×10^{-8}, irrespective of the mobile protocols or technology generation. Perhaps this requirement is the only constant across three technology generations.

A high percentage of the 2.3 million cell sites in service today depend on the TDM backhaul for their frequency source. Backhaul is the voice- and data-transport system between the cell tower and the centralized controller. Cell-phone users'

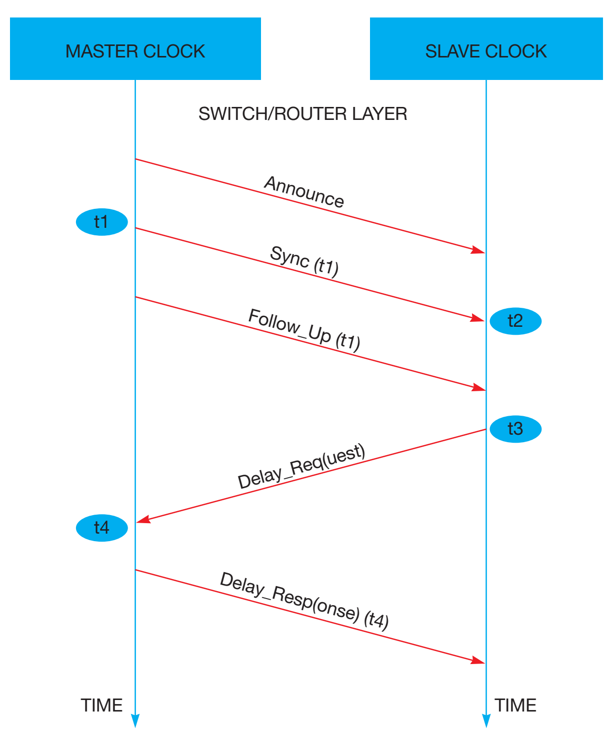

Figure 1 As part of the time-transfer process, the 1588 master and client devices exchange Sync and Delay_Req messages.

wide adoption of mobile broadband has led to a transition from TDM to Carrier Ethernet, isolating the base stations from their traditional clock reference. The industry cannot avoid the Ethernet migration, and it now requires a different but cost-effective method of delivering synchronization to base stations.

IEEE 1588 OVERVIEW

The IEEE created Version 1 of the 1588-2002 standard in 2002 to provide precision timing across LANs (local-area networks) for test-and-measurement and industrial-control applications. Segments of these industries needed to provide widely distributed sensors and actuators with a common time for coordinated measurement and control but without the need for an overlay timing infrastructure. The timing had to travel inband with the sensor traffic.

IEEE 1588 allows the accurate transfer of precision time from the master clock to the client clock through an asynchronous packet network. IEEE 1588 devices have a tree hierarchy, with the master clocks residing in centralized facilities and slave devices residing in remote locations that require time, frequency, or both. Note: This article uses the terms "grandmaster" and "server" interchangeably; it also uses the terms "client" and "slave" interchangeably.

An initiation process establishes a relationship between the server and the client. Next, a time-transfer process takes place (**Figure 1**). The 1588 master and client devices exchange Sync and Delay_Req messages. The messages contain the packet time of departure (t1, t3) and the time of arrival (t2, t4). The Sync message transports the time that it leaves the master.

It is difficult to know in advance the time when the packet will leave. In most cases, protocol designers add an optional second step. The two-step approach lets the Sync message transport the estimated value of t1; the Follow_Up message transports the actual value of t1, thus eliminating estimation errors. The slave uses t1, t2, t3, and t4 to calculate the round-trip delay and the clock offset—the difference between the server clock and the slave.

TABLE 1 MOBILITY AIR-INTERFACE-STABILITY NEEDS

Mobility standard	Frequency (ppb)	Time/phase
CDMA2000	50	<3 to <10 µsec
GSM	50	
WCDMA	50	
TD-SCDMA	50	3-µsec intercell phase change
LTE (FDD)	50	
LTE (TDD)	50	3-µsec intercell phase change
LTE MBMS	50	5-µsec intercell phase change
Backhaul	16	

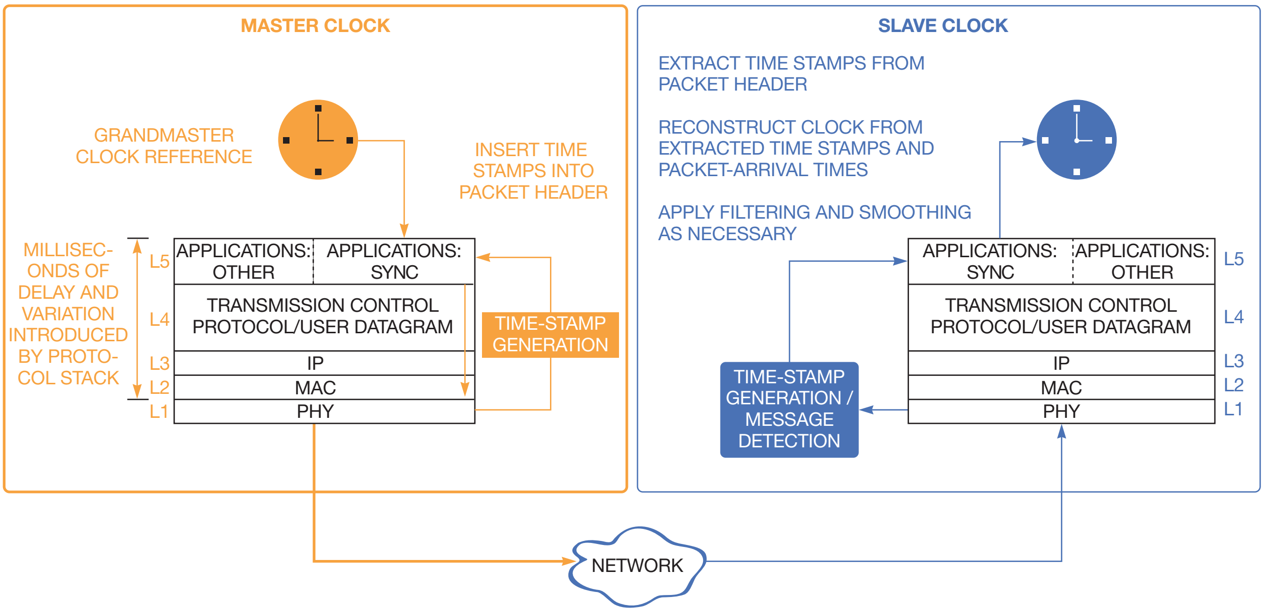

Figure 2 To avoid unpredictable stack-processing delays, the hardware time-stamps the packets at the PHY layer.

Assume that the one-way delay is half the round-trip delay. You can then determine the slave-clock offset using the following **equations**: (one-way delay)=[(t2–t1)+(t4–t3)]/2; slave offset=(t2–t1)–(one-way delay). You can now correct the slave-clock time using smoothing techniques and clock-offset values. A servo loop supports the recovery of frequency from the time-of-day clock. The process repeats multiple times a second, keeping the two clocks the same, or synchronized.

Therefore, the protocol assumes the path delay for the Sync messages is the same as that for the Delay_Req message—that is, the forward- and reverse-path delays are similar. In reality, this situation is not the case. By using frequent samples and smart disciplining algorithms, you can achieve telecommunication-compliant accuracies. To avoid unpredictable stack-processing delays, the hardware time-stamps the packets at the PHY (physical) layer (**Figure 2**). Packet jitter, or PDV (packet-delay variation), also affects clock-offset calculations.

PRECISION WITH 1588-2008

Version 1 of the 1588 protocol provided an effective method of distributing precise time over LANs, grabbing the attention of the telecommunications industry. Teaming with test-and-measurement and industrial-control partners, the IEEE developed a second version of the 1588 protocol to support WAN requirements. The result, IEEE 1588-2008, or PTP Version 2, includes a number of improvements to support the stringent needs of the telecommunications network. These improvements include higher message rates, hardware time-stamping, shorter message formats, unicast messaging, service reliability, and 1588 profiles.

The need for higher message rates arose to meet stability objectives. Using inexpensive client oscillators, the client must undergo more frequent updating. The revised PTP standard supports as many as 128 transactions/second, a large increase over the original maximum of one transaction/second.

Although the standard does not explicitly require hardware time-stamping, more frequent time-stamp updates have no value unless they are accurate. Hardware time-stamping on both the master and the client delivers the targeted submicrosecond accuracy.

To reduce the impact on network-bandwidth consumption, PTP shortened the original 165-octet (8-bit) message to 44 octets by placing information about the clock source and quality into a separate Announce message, which transfers less frequently.

The original standard supported only multicast message exchanges. IEEE 1588-2008 added support for unicast messaging. Unicast allows each client to listen to messages only from its master, reducing the processing power and cost of the client. More important, unicast messaging allows a unique relationship between the client and the server, supporting different synchronization messaging rates, inband status, and performance monitoring.

Carrier-class service means few outage minutes per year. In reality, some packet network paths experience occasional failures. L2/L3 networking takes care of rerouting the data, but interruptions in IEEE 1588 flows have a higher impact. IEEE 1588-compliant clients can select an alternative network grandmaster if the primary one fails.

The protocol specification aims to satisfy a range of applications and to achieve a specification with many options, including unicast and multicast. The IEEE created application profiles to ensure interoperability. Profiles define which options in the protocol specification clients must use. They also stipulate the interoperation of servers and clients that adhere to the profile definition.

IEEE 1588 defines only the default profile, which targets use in industrial-automation applications. The telecommunications industry has defined a telecom profile in the ITU-T (International Telecommunication Union-Telecommunication Standardization Sector) G.8265 recommendations. The protocol has defined new profiles, and compliance with the correct profile is as important as compliance with the overall specification.

IMPACT ON PERFORMANCE

The clock-recovery algorithm has the biggest impact on the performance of a 1588 system, but network behavior also defines the attainable performance. Packet delay, or latency; packet loss; and packet errors typically characterize network performance. These attributes, however, have almost no impact on packet-timing protocols.

The distinction is often blurry between managing the packet-network metrics and managing 1588 performance. Packet statistics are not sufficient for managing and reporting on the synchronization system. In addition to the network behavior, high-quality oscillators have an inherent stability that improves the quality of the output frequency and phase. Product designers must find a balance between the cost of the oscillator and the desired performance.

MAKING IT WORK

IEEE 1588 has the potential to become as ubiquitous as NTP (Network Time Protocol), but reaching that milestone means that multiple markets and applications will need to adopt it. The simplicity, scalability, and interoperability of the components will, however, define the extent to which 1588 will achieve that goal.

A time-and-frequency approach is only as good as its component parts. The origin of the time and frequency is the grandmaster clock (server). The IEEE 1588 time originates at the server and propagates through the network to the clients. Grandmaster clocks start with a good reference source, such as a GPS (global-positioning system) for time and frequency or a T1/E1 reference signal from a collocated primary reference clock. Because most server clocks now use GPS receivers, many industry participants consider IEEE 1588 as a distributed-GPS scheme. In addition to the source reference, grandmaster clocks should have high-quality oscillators to maintain accuracy if the system loses the reference for a time.

Grandmasters serve synchronized flows to many clients, so the serving capacity of the server is important. For example, a network with 300 clients using 64 transactions/second translates to a server capacity of 39,000 messages/second. The servers must hardware time-stamp the Sync and Delay_Req messages.

Because server clocks are so important, you must eliminate single points of failure. A high-quality server has redundant power supplies, redundant clocks, and network-interface protection. Wide deployment also means that you must be able to remotely monitor, manage, and upgrade the servers.

The server is central to synchronization, and it must be accurate, stable, and reliable. The client, however, has a tougher job. It lives at the end of the network and must contend with what is happening both in the cloud, including traffic levels, failures, and rerouting, and in the local area, including temperature changes and power-supply failures.

The fundamental choice for PTP Version 2 clients relates to oscillator quality, cost, and form factor. The better the client's local oscillator, the better it can handle whatever comes its way. However, better oscillators cost more, and reducing cost is the ultimate goal with the cellular-backhaul packet upgrade. The best PTP clients support as many as 128 messages/second and use hardware time-stamping to minimize induced jitter. The design of the oscillator servo is just as important to getting frequent low-jitter time stamps. The servo is the circuit in the PTP client that directs the oscillator to speed up or slow down after the reception of a new message. With good design of these factors, the best PTP clients can support cellular-backhaul frequency and time-reference requirements with low-cost oven-controlled crystal oscillators.

The best PTP Version 2 clients support the best-master-clock algorithm to reduce timing transients during path reroutes and unicast to allow the tuning of message rates for the best performance. Also, some network operators like to manually assign PTP clients to primary and backup grandmaster clocks. In this way, the operators will know the effect of network outages on each client. The best PTP clients allow this approach. Another feature of same-vendor PTP grandmaster-clock/client combinations is the ability of clients to report their performance status, enabling operators to conveniently monitor timing quality of service.

Monitoring servers is easy; users have for many years been managing similar devices over DCNs (data-communication networks) in centralized locations. But the timing community has never had to manage tens of thousands of devices, especially in situations in which they are beyond the reach of the DCN. In addition, client installations are at the ends of multiple VPN (virtual-private-network) links or on Ethernet segments that you cannot bridge to the DCN, and data connectivity between the client and element manager is impossible.

Monitoring the clients, whether external or embedded, must occur in telecommunication applications. Fortunately, the 1588 designers included management messages for inband management through the server. Element managers can access and monitor the installed clients through the server. Features such as client auto-discovery and bulk firmware upgrades allow the deployments to scale.

Simple deployment guidelines ensure the best 1588 results. First, select a high-performance, high-reliability grandmaster clock (server) that has the capacity for the number of clients you expect now and in the future. Second, select a high-quality 1588 client that works over the protocol in use—for example, native Ethernet, Ethernet over SDH (synchronous digital hierarchy), microwave, and xDSL. Embedded clients will become commonplace, but standalone clients reduce early deployment risks and serve the large installed base of legacy devices that can accept only the T1/E1-synchronized reference. The next step is locating the servers by determining the message rate of the server and the PDV that each client will experience. Cost considerations encourage the use of fewer servers functioning through more switches and routers, and robustness calls for the use of more servers with fewer links between the server and slave. The application will govern the balance between the two, with telecommunication networks favoring robustness. You can check the grandmaster's capacity by dividing the maximum transaction rate by the number of served clients and the number of transactions per second. If the demand exceeds the capacity, you can add modules or even grandmasters to share the load. Served clients are the clients that should routinely obtain synchronized flows from a grandmaster and those that could request the service if their grandmaster's clock fails. Finally, each client must have access to a backup grandmaster clock in the case of failure.

BEYOND TELECOM

IEEE 1588 is a new utility, and the network is the only limit on the applications for this utility. IEEE 1588 will work for any network-connected application, service, or device that needs time, frequency, or both. The industry will develop new 1588 profiles for different applications. Mobile-backhaul applications now have the largest interest in 1588 and should drive high-performance approaches that will operate over diverse and congested networks.

Other applications for IEEE 1588-2008 include industrial automation, distributed test and measurement, military deployments, and distribution of time to power-industry secondary plants. These examples are not exhaustive but demonstrate the wide applicability of IEEE 1588 beyond the telecommunications sector.

GETTING TO MARKET

Grandmasters will find wide deployment, and they typically work with small, half-rack 1588 clients—translators that convert IEEE 1588 synchronized flows to TDM signals. Embedding IEEE 1588 clients is a natural differentiator between similar products, and leading network-equipment manufacturers are integrating clients into their products.

Time to market is critical, and embedding third-party clients supports product differentiation and reduces development time. Clients are the most sophisticated elements of the technology, and you should leave the clock-recovery and servo algorithms to the specialists. Fortunately, soft clients and integrated chip modules are readily available for embedding into products.

It is important to note that PDV patterns are different for native Ethernet, microwave, and xDSL. Understanding the network is important when selecting third-party clients. Soft clients are typically more dynamic and easier to upgrade.

THE ROAD AHEAD

IEEE 1588-2008 is a viable means of distributing time over LANs and WANs, and it repairs the broken synchronization chains through packet networks. The protocol has reached specification maturity, and the road ahead involves simplifying the implementation of 1588. Focus areas for the short term include defining application-specific profiles and characterizing the behavior of physical layers on the end-to-end performance of the system. Building on that knowledge, you can expect high-performance autosensing algorithms for client devices. The industry will also focus on developing metrics that characterize a network's ability to support 1588, test tools to measure those metrics, and deployment and troubleshooting of the test tools.

IEEE 1588 is a new utility for distributing precise time and frequency over packet networks for a range of applications. With a considerable amount at stake, the telecommunications industry has led the way, particularly in the mobile-backhaul arena. Alternatives to 1588 exist, but no one-size-fits-all option exists. As a result, these options will find use in some areas of the network. IEEE 1588, however, exceeds the target of 16 ppb and meets the 3-µsec phase-accuracy goals over managed Ethernet, making it the preferred approach, particularly for the time-constrained TDD (time-division-duplex) and MBMS (multimedia-broadcast/multicast-service) modes of LTE (long-term-evolution) technology.

A lot has been learned from efforts in the telecommunications market, as reflected in the solution sets deployed in adjacent markets. Ultimately, product managers can differentiate products that depend on time, frequency, or both by embedding IEEE 1588 clients into their platforms. Proven off-the-shelf clients will allow engineering teams to meet R&D plans and deliver high-performance products. EDN

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AUTHOR'S BIOGRAPHY

André Marais is the director of business development for the wireless-market sector at Symmetricom Inc, where he helped develop the company's technology-training program. Previously, he served as a design engineer with Eskom, South Africa's power utility. Marais holds a bachelor's degree in electrical engineering and is a member of the South African Institute of Electrical Engineers.

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Set LEDs' hue from red to green

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

The circuit in **Figure 1**, which lets you create light of 32° of hues, uses red and green LEDs. A constant current divides into two components. One component flows through a red LED, and another one flows through a green LED. You can vary the current from 0 to 100% through the red LED, and thus you simultaneously vary the current through the green LED as a slave-type complement to 100%. When this scenario happens, your eye perceives the resulting light mixture as any hue between red and green. Roughly speaking, the transition from red to green passes through orange, amber, and yellow. You can set any of the 32 hues between red and green, passing through orange, amber, and yellow.

IC_3, an Analog Devices (www.analog.com) AD5228 resistive DAC, has one-in-32 resolution, and it thus sets the resolution of this circuit. In this application, the resistive DAC functions as a digital potentiometer. You can manually set its wiper position through short-term grounding of its $\overline{PU}$ pullup and $\overline{PD}$ pulldown control pins. The resistive DAC has no memory, so you have to make this setting after each power-on.

Holding the $\overline{PU}$ and $\overline{PD}$ pins to a logic low, the wiper position increments or decrements with an increased speed of one step per 0.25 sec, so the output light's color varies stepwise for a low pullup (**Figure 2**). You can also preset the hue of the LED, which appears at power-on. For a high Preset, the color is 100% red when you apply power. At a low Preset, a midposition is preset at the resistive DAC and thus

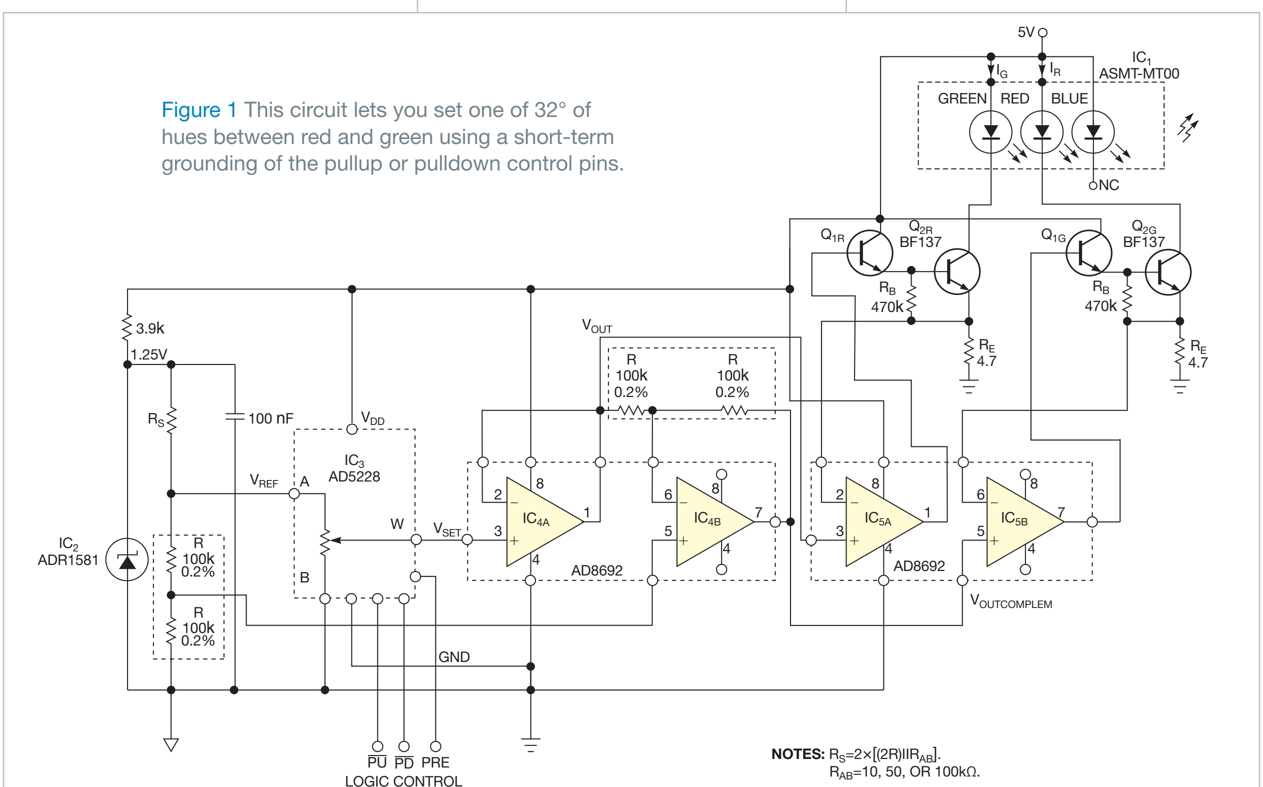

Figure 1 This circuit lets you set one of 32° of hues between red and green using a short-term grounding of the pullup or pulldown control pins.

the color at power-on is 50% red and 50% green; you perceive it as yellow.

The circuit uses two LEDs in IC_1, a high-performance, tricolor ASMT-MT00 LED from Avago Technologies (www.avago.com). The blue LED remains unused. You can, however, connect any of the remaining five red/green, red/blue, blue/red, green/blue, or blue/green combinations instead of the green/red combination this circuit uses.

Although the sum of currents flowing through the red and green LEDs is approximately one-fourth of the nominal per-LED current, the radiance is high, and you should not look directly at the lid of IC_1 when it is on from a distance of less than approximately 1 foot.

IC_2, IC_3, and IC_4 comprise a low-side source of two complementary analog voltages (**Reference 1**). The resistive DAC replaces the classic potentiometer in the earlier Design Idea. These complementary analog voltages are the input voltages for the two power stages comprising transistor Q_1 and midrange-power transistor Q_2.

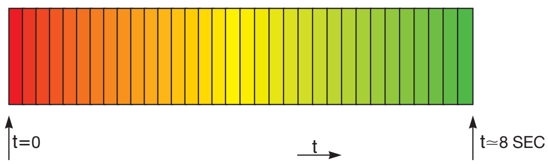

Figure 2 The light output changes quasicontinually from red to green within approximately 8 seconds, using long-term grounding of the pullup pin or a continuous grounding of the pin at power-on.

The power stage—voltage-to-current converters you make by cascading two bipolar transistors and an op amp—drives each of the two LEDs. The circuit senses output current at resistor R_E. The R_B resistors eliminate the leakage currents of both bipolar transistors in the cascaded series. These power stages would be functional even with one bipolar transistor instead of two. The cascaded bipolar transistors provide precision in the voltage-to-current converter. With a single power transistor, the relative error would be approximately $1/\beta$, whereas using the cascaded series, the error is approximately $1/(\beta_1\beta_2)$, where β_1 and β_2, the current gains of the bipolar transistors, are approximately 300 and 100, respectively. The error results from the current flowing through resistor R_E, which is the sum of the output current and the base current of transistor Q_1.

You can use this circuit in industries ranging from entertainment to toys; it may eventually find use in experimental psychology and in modern fine arts, which involves the use of optoelectronics.

Holding $\overline{PD}$ low and feeding a 50% duty cycle, 0.05-Hz-frequency logic waveform to the $\overline{PU}$ pin produces a slow, periodic, quasicontinuous "waving" of the color from red to green and back. EDN

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Circuit synchronizes sensors and cameras

By Shih-Jie Chou, Rui-Cian Weng, and Tai-Shan Liao,
National Applied Research Laboratories, Hsinchu, Taiwan

Measurement systems often use cameras and other sensors that require synchronization. This Design Idea describes an aerial-photography system that uses a camera comprising CCD (charge-coupled-device) image sensors, an inertial-measurement unit, and a GPS (global-positioning-system) unit. The resulting circuits provide trigger signals to synchronize the measurements at the optimal rate. The GPS provides information on spatial location, and the inertial-measurement unit provides information on spatial azimuth. The unit combines a gyroscope, a magnetometer, and an accelerometer to produce angular and acceleration measurements of a three-axis vector.

Figure 1 shows a system for taking aerial photographs. It comprises four Atmel (www.atmel.com) area-scan CCD image modules, one linear image-sensor module, two Dalsa (www.dalsa.com) PCI (Peripheral Component Interconnect) frame-grabber cards, the measurement unit, a clock-adjustment circuit, and a microcontroller. A Tektronix (www.tektronix.com) digital oscilloscope views the trigger signals during development.

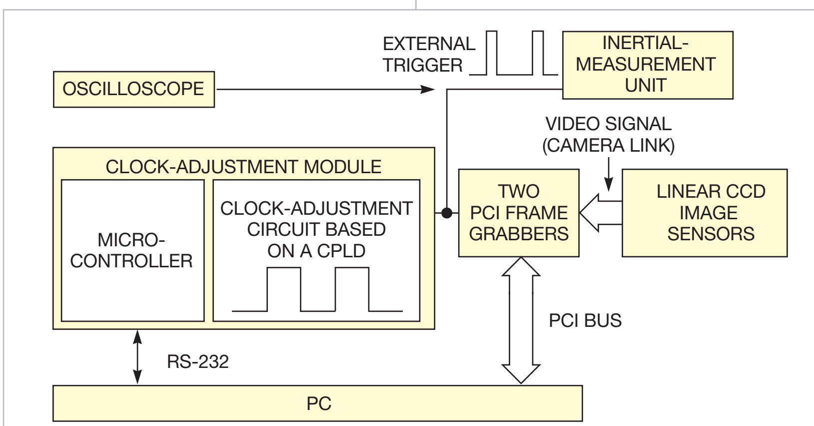

Figure 1 This clock-adjustment circuit generates a series of pulses that trigger the frame grabbers and the inertial-measurement unit.

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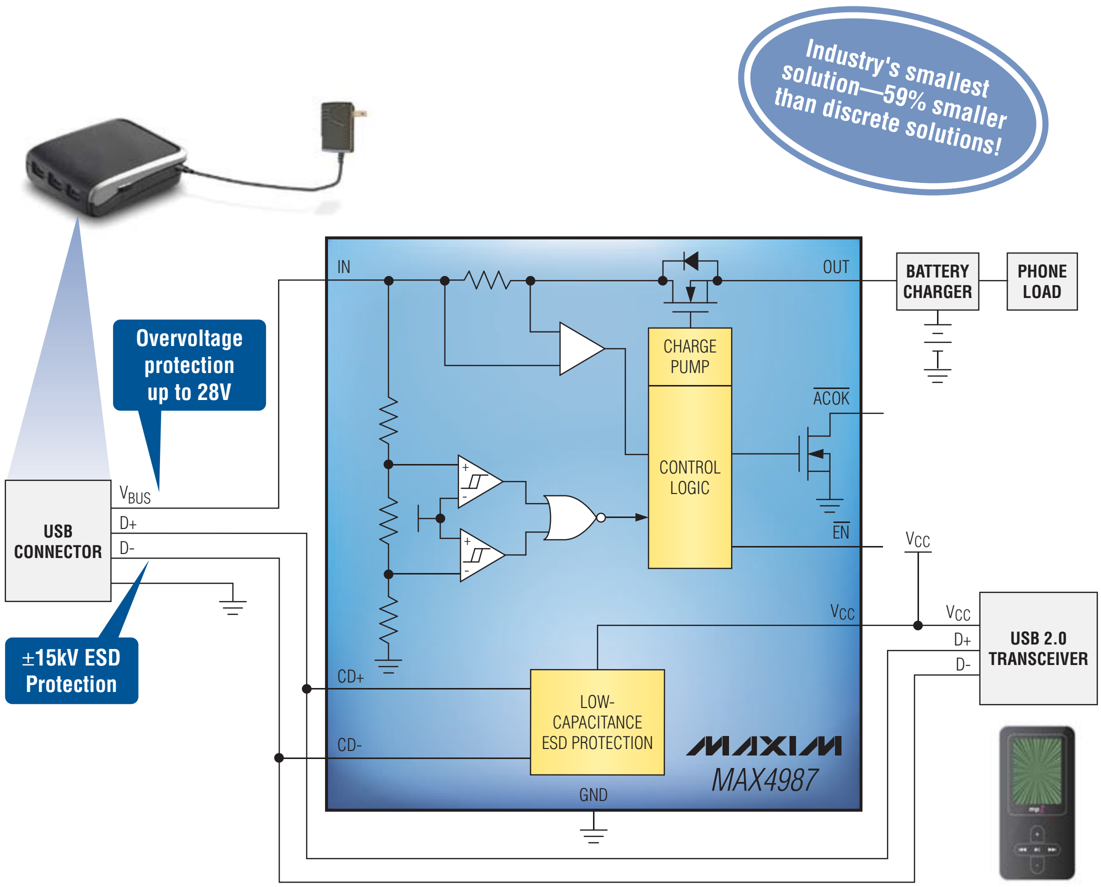

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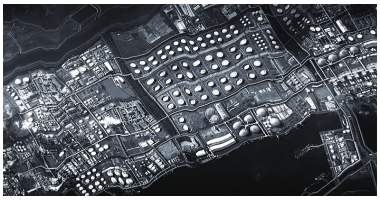


Figure 2 This aerial photograph from a height of 7000 feet was taken during a flight over Mailiao Township, Yunlin County, Taiwan.

The trigger signals that synchronize the sensors are the keys to this measurement system. The clock-adjustment circuit sends an external trigger pulse to the frame-grabber cards, which generate trigger signals for the system. Video modules comprising image sensors receive trigger signals from the frame grabbers. Each frame grabber captures an image and stores it in onboard memory before capturing the next image.

The external trigger pulses also control the sensors, GPS, and inertial-measurement unit. **Figure 2** shows a photo taken at 7000 feet in Mailiao Township, Yunlin County, Taiwan, using the external trigger circuit to drive and combine with the linear sensor and the measurement unit.

The circuit must change the external trigger clock's frequency to obtain the best frame rate. The CCD sensors that go into the linear-image-sensor module have 12,288 pixels, and each pixel measures 5×5 microns, producing images of approximately 500 lines/frame. The CCD image sensors have a maximum output rate of 320M pixels/sec. They use a Camera Link interface to send image data to the frame grabbers, which transfer the images to a PC over the PCI bus.

The clock-adjustment circuit generates the external trigger clock pulses. The circuit employs on an Altera (www.altera.com) CPLD (complex programmable-logic device) using Altera's development software to simulate the trigger signals and design the circuit. The clock-adjustment circuit provides as many as 15 trigger-signal frequencies to the system.

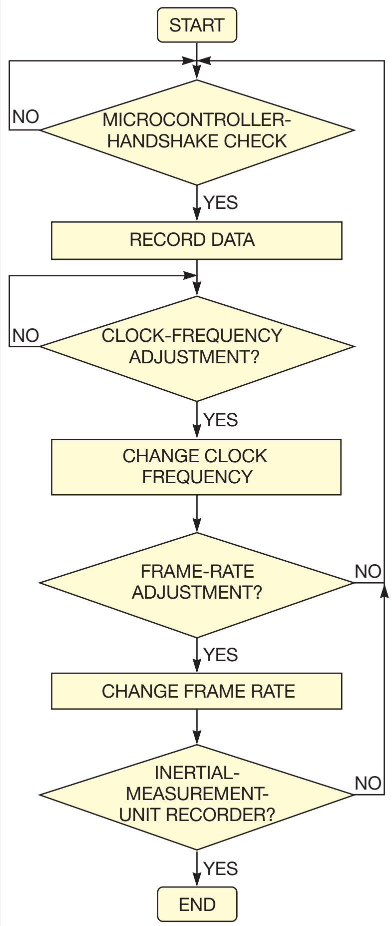


Figure 3 Microcontroller software adjusts the trigger-pulse frequency that drives the measurements.

The system's Atmel microcontroller contains 256 bytes of RAM and 8 kbytes of programmable flash memory for program storage. The microcontroller communicates to a PC over an RS-232 interface so that it can also receive commands and report its current state. This handshake process includes the decoding and encoding parameters for generating the trigger signal. The microcontroller also sends commands to the digital-timing-adjustment circuit; these commands change the pulse frequency of the external trigger.

You can adjust the frame rate of the CCD image module using 15 trigger frequencies. The external trigger signal also triggers the measurement unit to record and store spatial parameters. **Figure 3** shows the algorithm for finding the optimal trigger frequency. The frame rate and the trigger frequency are linearly proportional.

The inertial-measurement unit is a key sensor in the system, and there must be a direct correlation between it and the frame grabbers. If the external trigger frequency is 1 kHz, then each of the two frame grabbers captures 1000 frames/sec and the unit samples at 1k samples/sec. Through experimental results using aerial photography, the system successfully synchronizes all of the sensors.EDN

Circuit measures capacitance or inductance

Jim McLucas, Broomfield, CO

Engineers usually have access to signal and function generators, as well as frequency counters and oscilloscopes, but they may not have access to capacitance or inductance meters. Using the test setup in **Figure 1**, you can measure capacitance or inductance using a function generator, a multimeter, a frequency counter, and an oscilloscope.

Use the setup to measure the magnitude of two signals. You can then calculate the capacitance or inductance without measuring phase angles. You can express the ratio of input voltage to output voltage as:

$$\left|\frac{V_{IN}}{V_{OUT}}\right| = \frac{\sqrt{R^2 + X_C^2}}{X_C}, \qquad (1)$$

which you can put into the standard

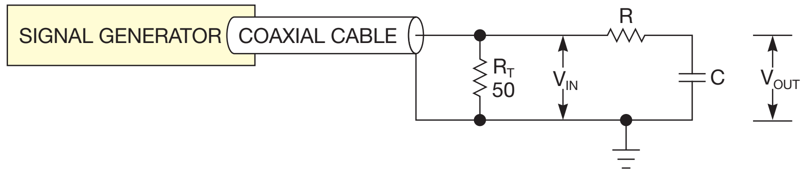


Figure 1 You can measure capacitance or inductance with this test setup.

form:

$$X_C^2+\frac{R^2}{1-\left|\frac{V_{IN}}{V_{OUT}}\right|^2}=0. \qquad (2)$$

After solving the **equation** for X_C, the result is:

$$X_C=\frac{R}{\sqrt{\left|\frac{V_{IN}}{V_{OUT}}\right|^2-1}}. \qquad (3)$$

Using the relationship

$$C=\frac{1}{2\pi f X_C}, \qquad (4)$$

the basic **equation** for capacitance is:

$$C=\frac{\sqrt{\left|\frac{V_{IN}}{V_{OUT}}\right|^2-1}}{2\pi f R}. \qquad (5)$$

Using the convenient ratio $|V_{IN}/V_{OUT}|=2$, then

$$C=\frac{\sqrt{3}}{2\pi f R}. \qquad (6)$$

To measure the value of a capacitor, measure the input voltage and then adjust the frequency of the signal generator to make the output voltage one-half of the input voltage. You need not use a 2-to-1 ratio for V_{IN}/V_{OUT}. You can just measure the input voltage and the output voltage and use one of the basic equations to calculate the value of the capacitance or inductance, but a ratio close to 2-to-1 is a good choice.

For best results, you can use a frequency counter to measure the frequency and a digital multimeter to measure the resistance. Most modern oscilloscopes can accurately measure the signals without loading the circuit, except for the capacitance of the probe. Capacitance is usually marked on the probe. Use the previous **equation** to calculate the value of the capacitor. Subtract the value of the probe capacitance from the result, and you have an accurate value for the measured capacitance.

USE A FREQUENCY COUNTER TO MEASURE THE FREQUENCY AND A DIGITAL MULTIMETER TO MEASURE THE RESISTANCE.

Usually, you know the approximate value of the capacitance you want to measure, so you can pick a starting value for the resistance, R, and the frequency, f, by using the following **equations**:

$$R=\frac{\sqrt{3}}{2\pi f C}, \qquad (7)$$

$$f=\frac{\sqrt{3}}{2\pi R C}, \qquad (8)$$

$$X_C=\frac{R}{\sqrt{3}}. \qquad (9)$$

You can use a similar procedure to measure inductance. In this case,

$$X_L=\frac{R}{\sqrt{\left|\frac{V_{IN}}{V_{OUT}}\right|^2-1}}, \qquad (10)$$

and the basic **equation** for inductance is expressed as:

$$L=\frac{R}{2\pi f\sqrt{\left|\frac{V_{IN}}{V_{OUT}}\right|^2-1}}. \qquad (11)$$

Set $V_{IN}/V_{OUT}=2$, then

$$L=\frac{R}{2\pi f\sqrt{3}}, \qquad (12)$$

$$R=2\pi f L\sqrt{3}, \qquad (13)$$

$$f=\frac{R}{2\pi L\sqrt{3}}, \qquad (14)$$

and

$$X_L=\frac{R}{\sqrt{3}}. \qquad (15)$$

For an example of measuring capacitance, assume C is approximately equal to 1000 pF and let f equal 1 MHz. Calculate as:

$$R=\frac{\sqrt{3}}{2\pi f C}=\frac{\sqrt{3}}{2\pi(10^6)(10^{-9})}=275.66\ \Omega. \qquad (16)$$

Use a 301Ω resistor or any convenient value of approximately 250 to 500Ω in the setup of **Figure 1**. Adjust the frequency while measuring the input voltage and the output voltage to get a ratio of 2-to-1. If the frequency you obtain is 912 kHz, the measured resistance of R is 304Ω, and the probe capacitance is 10 pF, then the capacitance is:

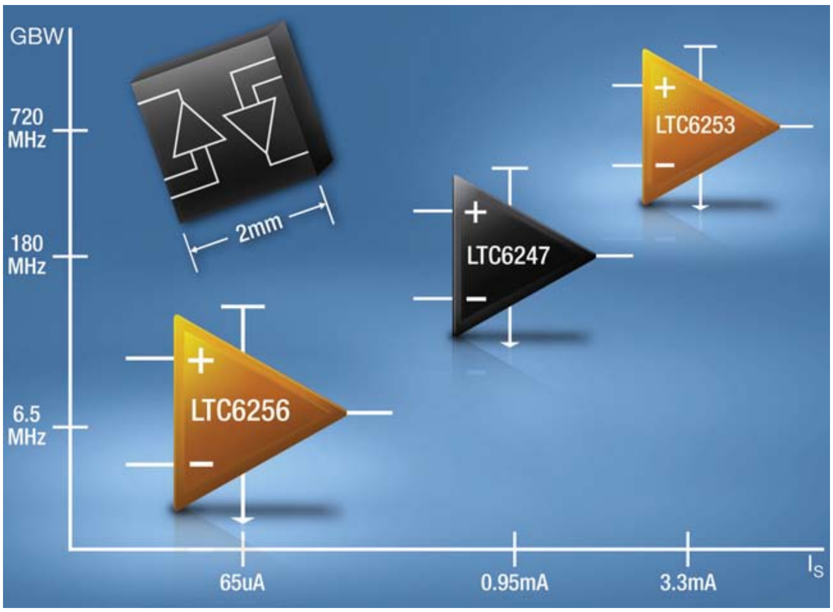
$$C=\frac{\sqrt{3}}{2\pi(912)(10^3)(304)}=994.3\ \text{pF}, \qquad (17)$$

minus 10 pF for the probe capacitance. The result is 984.3 pF.

The values for R and f are not critical; you should choose them to minimize parasitic effects. Resistance values of 300 to 3000Ω and frequencies of 100 kHz to 1 MHz should work. EDN

productroundup

AMPLIFIERS/OSCILLATORS/MIXERS



Op amps feature rail-to-rail operation

The silicon-germanium LTC6252/3/4 and LTC6255/6/7 single/dual/quad op amps achieve 720-MHz gain-bandwidth product and a 280V/µsec slew rate and consume a 3.3-mA supply current. The devices feature input-referred broadband noise of 2.75 nV√Hz, maximum input offset voltage of 350 µV at room temperature and a maximum of 1 mV at −40 to +125°C. They operate on 2.5 to 5.25V voltage supplies and have rail-to-rail inputs and outputs. They have a 42-µA power-down mode and a 90-mA output current. The LTC6253 is available in 2×2-mm DFN and SOT-23 packages. Prices start at $1.24 (2500).

Linear Technology Corp, www.linear.com

Low noise amp touts 90-MHz bandwidth at a gain of 10

The LMH6629 features 0.69-nV/√Hz noise with a −3-dB bandwidth of 900 MHz at a gain of 10. Targeting use in communications, test-and-measurement, medical-imaging, industrial, and light-detecting-and-ranging applications, the amplifier also has 2.6-pA/√Hz input-current noise and second- and third-harmonic distortion of −90 and −94 dBc, respectively. Maximum input offset voltage is 780 µV at 25°C and ±0.45 µV/°C of offset-voltage temperature compensation. The unit's common-mode range extends below ground, and the output swings to within 0.8V of either rail with an output current greater than ±250 mA. The op amp consumes 15.5 mA and has a supply-voltage range of 2.7 to 5.5V. Designers can set a minimum gain of four or 10 by pulling the minimum-gain-select pin low or high. The device employs the vendor's CBiCMOS8 silicon-germanium process technology. It comes in an eight-pin LLP, operates over a temperature range of −40 to +125°C, and sells for $1.88 (1000).

National Semiconductor, www.national.com

Fully differential op amp drives 16-bit ADCs

The 26-bit, fully differential THS770006 op amp features full-scale precision to 200 MHz for wireless-base-station, high-speed-data-acquisition, test-and-measurement, medical-imaging, and defense applications. The device offers a third-order intermodulation distortion of −107 dBc at 100 MHz and a 7.5-nsec overdrive recovery. The device comes in a 4×4-mm QFN-24 package, and prices start at $4.10 (1000). The THS770006EVM (evaluation module) is also available now and sells for $99.

Texas Instruments, www.ti.com

Low-power op amps extend battery life

The MCP6401/2/4 op amps feature quiescent current of 45 µA with a gain-bandwidth product of 1 MHz. Maximum offset voltage is ±4.5 mV, and supply voltage ranges from 1.8

to 6V over a −40 to +125°C temperature range. The unity-gain-stable devices also feature rail-to-rail input and output operation. Four evaluation boards are also available for $30 each. The MCP6401/1U/1R op amp comes in five-pin SC-70 and SOT-23 packages and sells for 26 cents (10,000), and the MCP6402 op amp comes in eight-pin SOIC and 2×3-mm TFDN packages and sells for 32 cents (10,000).

Microchip Technology, www.microchip.com

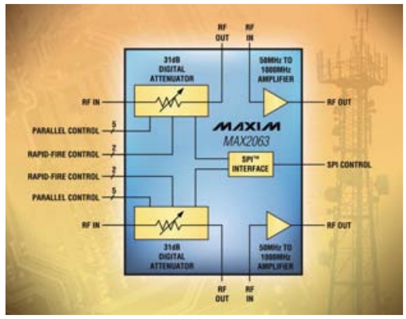
Thermocouple amplifiers integrate cold-junction compensation

The AD8494 thermocouple amplifiers for K- and J-type thermocouples feature on-chip cold-junction compensation that automatically adjusts the thermocouple's output for changes in ambient temperature. The device, which converts the small voltages from a thermocouple junction to a 5-mV/°C analog signal, has a common-mode rejection of 0.1°C/V, operates from single 2.7V to dual ±18V supplies, and consumes 18 µA of quiescent supply current. With a 5V supply the AD8494 can cover nearly 1000° of a thermocouple's temperature range. The device comes in an eight-lead MSOP, operates at 0 to 50°C, and sells for 98 cents (10,000).

Analog Devices Inc, www.analog.com

VGA claims 32% footprint reduction

The fully programmable, multistate, dual-channel, digital IF/RF MAX2063 VGA (variable-gain amplifier) provides four customized attenuation states per path, 25-nsec digital switching, and low digital-VGA-amplitude overshoot and undershoot. It targets use in automatic-gain-control circuits in 2.5, 3, and 4G wireless-infrastructure transceivers, including GSM/EDGE, CDMA, WCDMA, LTE, and WiMax applications. The MAX2063 can serve as either an IF or an RF VGA and has a 50- to 1000-MHz frequency range. Cascaded linearity for output third-, second-, and first-order intercept points is 41, 56, and 19 dBm, respectively. Second- and third-order harmonic distortion is −54.8 and −72.9 dBc, respectively. The MAX2063 comes in a 48-pin TQFN package and sells for $6.90 (1000).



Maxim Integrated Products, www.maxim-ic.com

EDN ADVERTISER INDEX

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Bet your boots: It's beer time!

DANIEL VASCONCELLOS

In the late 1970s, I was working for an NBC (National Broadcasting Co) affiliate in Champaign, IL. Much of our equipment employed vacuum tubes that were so hot that we used them to warm up sandwiches. Our air-conditioning expenses were high, but our heating bills were low. One piece of equipment, a vacuum-tube-based, 2-in. video recorder, was especially good at minimizing our heating bills.

The assistant chief engineer, "Hank," was concerned about the amount of heat this recorder put out, so he added a fan to accelerate the heat removal and to direct the hot air past his wet galoshes after slogging through the slush from the parking lot. Unfortunately, the VR2 measured approximately seven feet high, providing a powerful chimney effect that just about matched the power of the fan that Hank had installed.

We noticed that Hank's galoshes were still wet when he put them on at "beer time": 4:30 p.m. Why wasn't our "boot dryer" working? After a couple of days, we found that the trace of the oscilloscope monitoring the equipment would drift up and off of the screen after the VR2 had been on for a while. This movement made it difficult for us to keep video levels where they needed to be. We reversed the fan and put Hank's boots on a step ladder near the air exit at the top of the VR2. Come beer time, his boots were toasty dry, and the oscilloscope trace temporarily quit drifting.

Hank pulled out the lab scope to troubleshoot the problem. After a few nights, I noticed that Hank was looking more tired and frazzled than usual and that the VR2 oscilloscope trace was still drifting. I asked Hank whether he was going to be able to fix the VR2 scope; the other engineers were complaining that it was a nuisance. "Why don't you take a look at it?" he asked. I had perused the manual, so I knew that the scope's vertical-deflection circuitry was a symmetrical push-pull type. I thought that I should be able to exchange tubes from the top to bottom and easily isolate the problem. The tube exchange didn't pan out, however. After a couple of evenings, I, too, was becoming frazzled. Hank, on the other hand, was looking more relaxed.

After my third or fourth evening of frustration and a few cans of "component-cooling spray," I was driving home when I suddenly had an epiphany. Being well into my 20s, I'd previously had a couple of other epiphanies, so there was not much danger of having an auto accident because of it. I recalled that, while watching the grid voltage on the vertical-deflection drivers as the signal was drifting up, both grids did what they were supposed to be doing: centering the display signal. The layout of the circuits made it difficult to directly observe the signal on the grid, so I had been looking at it on the side of the grid resistor away from the grid. I had no inclination that I would see anything different on the grid side—that is, until I had the epiphany. The next evening, I made a minor modification to the circuit to allow me to directly see the grid.

The voltage on the grid was going in the opposite direction from the voltage on the other side of the grid resistor. I exchanged the upper and lower driver tubes and verified that the phenomenon did not follow the tube but was always in the upper deflection circuit. It turned out that the excess heat from the failed galoshes-drying experiment had permanently changed both driver tubes. Because of the physical placement and orientation, they would now fail only when they were in the upper part of the deflection circuit. In the upper circuit, the grid would heat up so much that it would emit electrons as if it were a cathode. This current flow caused the voltage on the grid side of the resistor to rise, enhancing plate-current conduction.

The next day, Hank gave me a set of tubes to try. I put them in, and the drifting signal drifted no more. EDN

David Porter of Columbus, IN, is an engineer with a First Class Federal Communications Commission License with radar endorsement.

+ www.edn.com/tales